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Artificial Neural Networks and Hybrid Evolutionary Algorithms for Multi-Objective Optimization of Analog Integrated Circuit Design

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***Abstract*-The design of analog integrated circuits demands the careful optimization of multiple interdependent parameters, including transistor sizes, bias currents, and passive components, to meet stringent performance targets such as gain, bandwidth, phase margin, and power efficiency. To address this challenge, this work introduces a computational intelligence framework that combines artificial neural networks (ANNs) with a hybrid genetic algorithm–particle swarm optimization (GA–PSO) strategy. The framework was validated on two representative circuits: a two-stage CMOS operational amplifier with Miller compensation and a differential LC voltage-controlled oscillator (LC-VCO) operating at 2.8 GHz in 0.18-µm CMOS technology. Extensive HSPICE simulations generated datasets that enabled the ANN to capture the complex nonlinear relationships between design variables and performance metrics. The method successfully predicted optimal device dimensions and biasing conditions, achieving a 160% improvement in figure of merit (FoM) for the amplifier and a FoM of 118.1 dBc/Hz for the LC-VCO, comparable to state-of-the-art designs. These results demonstrate the framework's versatility and scalability, providing a flexible soft-computing tool for multi-objective optimization across diverse analog circuit topologies.**

***Index Terms*- Analog IC performance, Computational intelligence, Optimization algorithms, Circuit simulation, HGAPSO**

I. INTRODUCTION

Analog circuits play a crucial role in a wide range of applications, including wireless communications, biosensors, and numerous other fields [1–4]. Traditionally, the design parameters of analog circuits, such as transistor dimensions and biasing conditions, have been determined manually by designers based on experience and domain knowledge. This trial-and-error approach is not only time-consuming but also does not necessarily guarantee optimal designs. Moreover, due to the inherent trade-offs among circuit parameters, improving one performance metric can often lead to the degradation of another, making it challenging to satisfy stringent specifications. Consequently, with the growing demand for low-power, high-performance integrated circuits, adopting automated design methodologies has become increasingly important.

In recent years, artificial neural networks (ANNs) and evolutionary algorithms have emerged as powerful tools for optimizing analog circuit design [5–6]. Neural networks, owing to their parallel architecture, can perform high-speed computations that significantly reduce design time, while their adaptive nature allows them to be trained on input–output data and adjust to variations [7]. Simultaneously, advanced optimization techniques—including ant colony optimization [8–9], grey wolf optimization [10], genetic algorithms [11–12], differential evolution [13–14], and simulated annealing [15–16]—have been increasingly applied to determine optimal design parameters. Despite their advantages, these methods often face limitations such as slow convergence and a high risk of being trapped in local optima, preventing achieving globally optimal solutions. This work investigates the capability of a hybrid Genetic Algorithm–Particle Swarm Optimization (GA–PSO) framework in training neural networks to design analog circuits, generate

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novel designs, and enable user-defined trade-offs among multiple design parameters. To demonstrate the generalization potential of the proposed framework, Validation Examples are provided, encompassing Validation Example I: Two-Stage CMOS Operational Amplifier and Validation Example II: Differential CMOS LC Voltage Controlled Oscillator (LC-VCO), illustrating its applicability across diverse analog circuit topologies. The remainder of the paper is organized as follows: Section 2 briefly reviews the application of neural networks in automated analog circuit design. Section 3 introduces the hybrid GA–PSO algorithm, while Section 4 details its use in neural network training. Section 5 presents validation examples of representative analog circuits. Section 6 discusses dataset generation via parallel HSPICE simulations, and Section 7 addresses data preprocessing for effective ANN training. Section 8 elaborates on neural network architecture selection and training, demonstrating the generation of new circuit designs and management of trade-offs among performance metrics. Finally, Section 9 provides a comparative analysis of the proposed methodology against existing approaches, highlighting its efficiency and versatility, followed by concluding remarks.

II. Application of Neural Networks in Automated Analog Circuit Design

As previously outlined, the design of analog circuits—particularly operational amplifiers necessitates profound expertise to comprehend the intricate and nonlinear relationships that exist between design parameters and circuit performance metrics, alongside establishing optimal trade-offs tailored to specific application requirements. As depicted in Fig. 1, variations in a single design parameter can exert direct or indirect effects on multiple performance characteristics, often in conflicting manners. For instance, an increase in supply voltage typically reduces input-referred noise, yet concurrently escalates the overall power consumption of the circuit.

Traditional intelligent analog design methodologies rely heavily on sophisticated physics-based formulations or detailed circuit-level simulations to model the complex interplay between design variables—such as transistor channel width and length—and key performance indicators including gain, power consumption, and gain–bandwidth product. However, to alleviate the complexity of these models, numerous physical and electronic phenomena are frequently omitted, which inevitably compromises the accuracy and reliability of the resultant designs.

In contrast, artificial neural networks (ANNs) offer a robust framework capable of addressing multivariate design challenges by directly mapping design inputs to performance outputs without explicit reliance on complex analytical equations. Moreover, once adequately trained, these neural models facilitate the generation of diverse circuit designs conforming to user-defined specifications. Consequently, the highly nonlinear and multidimensional characteristics inherent to analog circuit performance can be effectively encapsulated by training ANNs on sufficiently extensive and high-quality datasets.

Upon completion of training, the ANN can inversely infer optimal design parameters based on desired performance targets, thereby streamlining the analog design process [17].

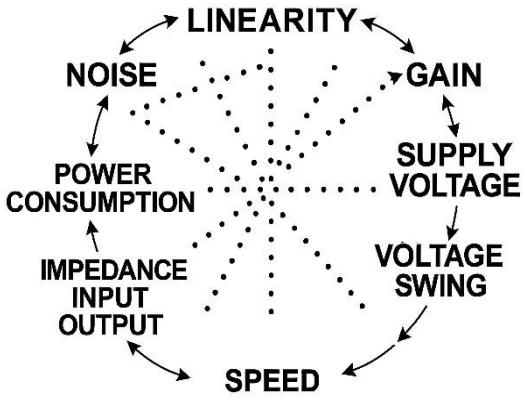

Fig 1. Complicated and nonlinear relation of analog circuit performance parameters

III. Hybrid Genetic–Particle Swarm Optimization Algorithm (HGAPSO)

The Hybrid Genetic–Particle Swarm Optimization (HGAPSO) algorithm is developed by integrating the Genetic Algorithm (GA) with Particle Swarm Optimization (PSO). Given that both methods draw inspiration from natural phenomena, their foundational principles are first elaborated before introducing the hybridization approach.

A. Genetic Algorithm (GA)

The Genetic Algorithm (GA), originally proposed by John Holland in 1975 at the University of Michigan, is grounded in the principles of genetics and Darwinian evolution, fundamentally relying on the concept of "survival of the fittest" or natural selection. Among its prominent applications is its use as an optimization technique. GA has been extensively utilized in various fields such as pattern recognition, feature selection, image processing, and machine learning [18–19]. Conceptually, GA is a population-based stochastic search and optimization method inspired by natural genetic processes, aiming primarily to minimize a given cost or objective function. Unlike traditional optimization methods that initiate the search from a single solution, GA explores the search space starting from an entire population, thereby enhancing the probability of locating the global optimum. The operation of GA revolves around three core genetic operators:

- **Selection**
- **Crossover**
- **Mutation**

The selection operator is responsible for choosing individuals from the current population to form a new generation. This choice is predominantly influenced by the fitness value of each individual, where higher fitness correlates with a higher likelihood of selection. The probability P_i of selecting the i_{th} individual is computed as follows:

$$P_i = \frac{F_i}{\sum_{j=1}^{popsize} F_j} \quad (1)$$

Where F_i denotes the fitness value of the i_{th} individual and N is the population size. New generations are produced via the crossover and mutation operators, which are applied with

probabilities P_c and P_m, respectively. The iterative process continues until termination criteria are satisfied, such as reaching a predetermined maximum number of generations or achieving convergence indicated by a stable standard deviation in the population's fitness values.

B. Particle Swarm Optimization (PSO)

Particle Swarm Optimization (PSO) was first proposed by Kennedy and Eberhart in 1995 [20]. Similar to other population-based evolutionary algorithms, PSO initializes with a randomly generated population of candidate solutions, referred to as "particles." Each particle navigates the search space by iteratively updating its position based on its velocity, guided both by its individual best-known position (Pbest) and the global best position (Gbest) discovered by the swarm.
Consider a search space of dimension D, where the state of each particle is described by its position vector $X_i$and velocity vector V_i. The position and velocity of each particle at iteration t+1 are updated according to the following equations:

$$V_i^{t+1}=wV_i^t + C_1r_1(Pbest_i - X_i^t) + C_2r_2(gbest_i - X_i^t) \quad (2)$$

$$X_i^{t+1} = X_i^t + V_i^{t+1} \quad (3)$$

Where V_i^{t+1} and V_i^t represent the updated and current velocity vectors of particle i, respectively; X_i^t and X_i^{t+1} denote the current and updated positions. The term Pbesti corresponds to the best position found individually by particle i, whereas Gbest signifies the best position identified by the entire swarm. The coefficients C_1 and C_2 are the cognitive and social acceleration factors, typically set within the range of 1 to 2. The stochastic variables r_1 and r_2 are uniformly sampled from the interval [0, 1]. The inertia weight w, usually assigned a value between 0.4 and 0.7, modulates the trade-off between global exploration and local exploitation.

C. Hybrid Genetic–Particle Swarm Optimization Algorithm (HGAPSO)

As previously discussed, the Particle Swarm Optimization (PSO) algorithm offers advantages such as rapid convergence and the ability to perform both global and local searches in parallel, maintaining an effective balance between exploration and exploitation. These characteristics can be leveraged to mitigate the issue of premature convergence typically observed in Genetic Algorithms (GA), thereby improving the quality of the selected parents. Consequently, the integration of GA and PSO forms a mutually complementary framework [21]. The HGAPSO algorithm operates based on this principle [22]. It starts with a randomly initialized population, and after evaluating the fitness of all individuals, the top 50% with the highest fitness scores—referred to as elites—are selected. These elite individuals then undergo refinement using the PSO mechanism. The PSO-driven enhancement process improves the quality of the elites, producing higher-quality offspring in subsequent generations and enhancing the algorithm's exploratory capabilities.

In the final phase, the optimized elite individuals are directly transferred to the next generation, while the rest of the population is generated through traditional GA operations such as crossover and mutation. The overall workflow of the HGAPSO algorithm is depicted in Fig. 2.

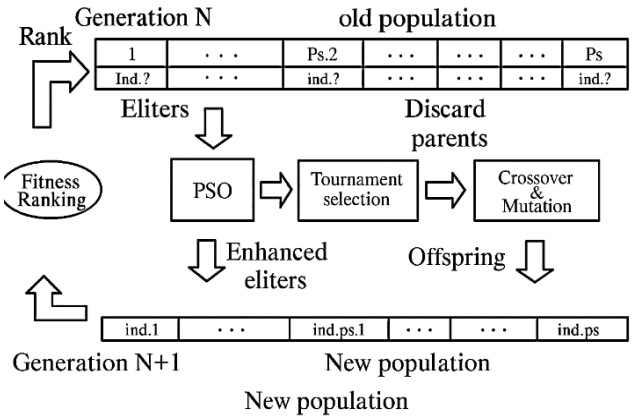

Fig2. The implementation procedure of the HGAPSO algorithm

IV. Neural Network Training via the HGAPSO Algorithm

In neural network training, the primary optimization parameters are the weights and biases associated with each neuron. If the *i*th layer of the network contains *V* input nodes and *N* neurons, the corresponding weight matrix W^i and bias vector B^i are defined as shown in (4):

$$W^i = \begin{bmatrix} (w_1^i)^t \\ (w_2^i)^t \\ \cdot \\ \cdot \\ \cdot \\ (w_n^i)^t \end{bmatrix} \qquad B^i = \begin{bmatrix} b_1^i \\ b_2^i \\ \cdot \\ \cdot \\ \cdot \\ b_n^i \end{bmatrix} \quad (4)$$

In this study, the optimal values for these parameters are obtained using the HGAPSO algorithm. The procedure begins by initializing the weights and biases of all neurons with random values. The neural network is then executed using these initial values, and the resulting error from each forward pass is used as the fitness value to evaluate each candidate solution.
Subsequently, the HGAPSO algorithm updates the weights and biases based on its evolutionary equations. This iterative training process continues until either a predefined error threshold is met by one of the individuals or a stopping criterion (such as the maximum number of iterations) is reached. Upon completion of the training phase, the final optimized weights are used to compute the classification error on the training dataset. The same set of weights is then applied to evaluate the model's performance on the test dataset.

V. Validation Examples of Representative Analog Circuits

A. Validation Example I: Two-Stage CMOS Operational Amplifier

Validation Example I describes a two-stage CMOS operational amplifier incorporating a PMOS differential input pair along with Miller compensation, as shown in Fig. 3. In this design, the positive and negative supply voltages (V_{DD} and V_{SS}) are set to +3.3 V and –3.3 V, respectively. Furthermore, the DC bias voltages applied to the differential

input terminals $Vin_+$and Vin_- are both maintained at 0.8 V, ensuring symmetric operation and stable amplifier performance.

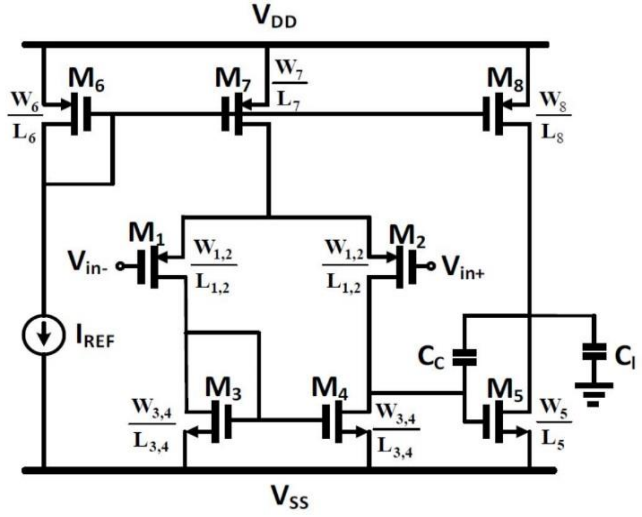

Fig 3. Miller compensated two-stage operational amplifier

Furthermore, to prevent a mismatch in the differential pairs, the channel widths and lengths of transistors M_1 and M_2, as well as M_3 and M_4, are set to be identical. Accordingly, a sample design parameter vector V_i is defined as in (5):

$$V_i = [W_{1,2}, W_{3,4}, W_5, W_6, W_7, W_8, L_{1,2}, L_{3,4}, L_5, L_6, L_7, L_8, I_{REF}, C_C, C_l] \quad (5)$$

Where W and L represent the channel width and length of the transistors, respectively. I_{REF} denotes the reference current source, C_C is the compensation capacitor, and C_l represents the load capacitor. Four key parameters are considered to evaluate the performance of the operational amplifier: low-frequency gain, power consumption, phase margin, and the gain–bandwidth product.

B. Validation Example II: Differential CMOS LC-VCO

To further evaluate the generalization capability of the proposed ANN + GA–PSO framework, a second validation example was conducted on a differential CMOS LC voltage-controlled oscillator (LC-VCO) operating at 2.76 GHz in a 0.18-µm CMOS technology. The oscillator is based on a Colpitts-inspired topology with capacitive feedback from the gate to the source, which provides high negative trans conductance and ensures reliable start-up even at low bias currents. To enhance negative trans conductance and achieve stable oscillation, the circuit incorporates cross-coupled PMOS transistors along with a differential LC tank. Key performance parameters, including negative trans conductance, oscillation frequency, and phase noise, were carefully analyzed and optimized [23]. The schematic of the designed LC-VCO is shown in Fig. 4.

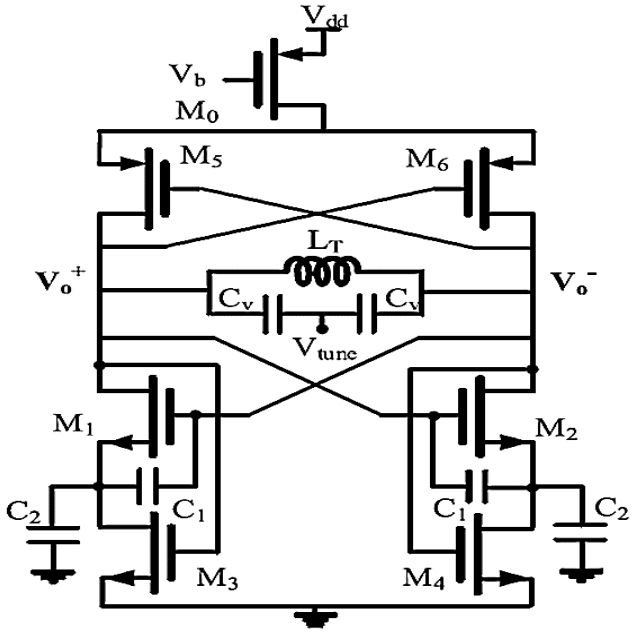

Fig 4. The differential LC voltage-controlled oscillator (LC-VCO)

In this design, the output frequency is controlled via a tuning voltage V_{tune}, which is applied to accumulation-mode varactors. The applied tuning voltage modifies the varactors' capacitance, thereby adjusting the oscillator's frequency. These varactors enable precise frequency control, making the LC-VCO highly tunable and suitable for high-performance analog applications. Based on this, a sample design parameter vector V_i is defined as shown in (6):

$$V_i = [\mathrm{W/L_{1,2}}, \mathrm{W/L_{3,4}}, \mathrm{W/L_{5,6}}, L_T, C_V, C_1, C_2] \quad (6)$$

VI. Data Acquisition from Analog Circuit Performance

One of the major challenges in leveraging artificial neural networks for automated analog circuit design lies in obtaining a representative and high-quality dataset from the complex performance landscape of analog circuits, which is essential for effective neural model training. Previous studies have employed various strategies for dataset generation, including intelligent and adaptive sampling within the design space [24–29], extracting data from ongoing optimization algorithm executions [30], and selecting feasible initial points followed by parameter variation in their vicinity [31].

In this work, a two-step sampling approach is adopted. First, a global random search is conducted to identify initial points across the entire design space, followed by localized sampling around these points through small perturbations to enhance sampling density and reduce computational overhead. The design space boundaries defined by the minimum and maximum allowable values of critical design parameters, such as transistor dimensions and reference current sources, are set based on technological and design constraints, as detailed in Table I.

For the initial global search, 1000 random design points are generated per iteration within the specified parameter ranges. This process yields a 15×1000 matrix, where each row corresponds to a distinct set of 15 design parameters. Each candidate design is then simulated using HSPICE on the two-stage operational amplifier model depicted in Fig. 3. All circuit simulations were conducted using HSPICE version 2021.09, under the typical–typical (TT) process corner, and at a nominal temperature of 25 °C. Four key performance metrics are extracted for each design point: low-frequency gain, power consumption, phase margin, and gain–bandwidth product. Next, acceptable ranges for average performance metrics are defined (see Table II), and design points outside these thresholds are discarded to focus on regions with moderate yet meaningful performance levels, thereby accelerating dataset collection. This phase continues until 100 acceptable initial points are identified. Subsequently, the design parameters around each point are iteratively varied by up to 30%, and any newly generated acceptable points are added to the reference set for further neighborhood exploration. This iterative refinement continues until 8000 valid design points are collected.

To ensure a balanced representation of the design space, we employed a two-step sampling approach, followed by a dedicated evaluation of potential dataset bias. While the initial sampling focused on points within acceptable performance ranges to accelerate data collection, supplementary experiments were conducted in which a subset of low-performance points was deliberately included. This allowed the ANN to capture broader design relationships, and the results confirmed that the network's predictions remain stable and robust, demonstrating effective generalization across the design space.

Finally, an outlier removal step is performed, whereby any design point exhibiting deviations exceeding three standard deviations from the global mean (computed over all 8,000 samples) in any of the key performance metrics is excluded. This filtering reduces dataset variance and improves the quality and robustness of neural network training. In this study, parallel processing was employed in HSPICE to accelerate sampling and reduce the overall design process time. The computations were carried out on a workstation with 16 GB of RAM and a quad-core Intel processor operating at a maximum clock speed of 2.4 GHz, which reduced the total sampling time for data collection to 37 minutes and 43 seconds.

TABLE I
Design Parameters and their Acceptable Ranges

Design Parameter	Minimum (μm)	Maximum (μm)	Design Parameter	Minimum	Maximum
$W_{1,2}$	0.18	200	W_7	0.18 (μm	200(μm)
$L_{1,2}$	0.18	3	L_7	0.18(μm)	3(μm)
$W_{3,4}$	0.18	200	W_8	0.18(μm)	200(μm)
$L_{3,4}$	0.18	3	L_8	0.18(μm)	13(μm)
W_5	0.18	200	I_{REF}	0.1 (μA)	120(μA)
L_5	0.18	3	C_l	0.001(pF)	10 (pF)
W_6	0.18	200	C_C	0.001(pF)	10 (pF)
L_6	0.18	3	----	----	----

TABLE II
Performance Parameters and their Acceptable Ranges for Training Dataset

Performance Parameter	Minimum	Maximum
Low-frequency gain	40 dB	60 dB
Power consumption	0.1 mW	10 mW
Phase margin	55	100
Gain–bandwidth product (GBW)	0.01 MHz	10 MHz

Similarly, the same procedure was used to acquire data from the LC-VCO, generating 1000 random design points per iteration within the predefined parameter ranges. This produced a 7×1000 matrix, each row representing a unique combination of seven key design parameters. Four main performance metrics—oscillation frequency, power consumption, phase noise, and the figure of merit (FOM), detailed in Section 9—were carefully evaluated to facilitate meaningful comparisons with recent designs.

VII. Data Normalization

Following the extraction of input and output datasets from HSPICE simulations, the subsequent step in the modeling pipeline involves data normalization to standardize the dataset for effective neural network training. Given the considerable disparity in the scales of design variables and performance metrics—for example, transistor widths measured in micrometers versus DC gain expressed in decibels—normalization is imperative to mitigate scale-induced bias and facilitate the convergence of the training algorithm. In this work, a min-max normalization technique is applied to rescale all variables within the interval [0, 1], as formalized in (7):

$$x_{norm} = \frac{x - x_{min}}{x_{max} - x_{min}} \quad (7)$$

Where x denotes the original data value and x_{norm} represents the normalized output.

VIII. Structure of the Artificial Neural Network and Training Procedure

In the present work, a feed-forward multilayer perceptron (MLP) comprising two hidden layers is employed to model the performance characteristics of the operational amplifier under investigation. The neural network is developed using MATLAB's Neural Network Toolbox. The input layer consists of 15 neurons, each corresponding to specific design parameters including the transistor width-to-length (W/L) ratios, bias current, and values of compensation and load capacitors. The architecture features two hidden layers: the first with 10 neurons and the second with 7 neurons, both utilizing the sigmoid activation function to introduce nonlinearity. The output layer comprises four neurons, each representing a key circuit performance metric: low-frequency gain, unity-gain bandwidth (GBW), power consumption, and phase margin. A linear activation function is adopted in the output layer to facilitate accurate prediction of continuous output values. Training is conducted using a hybrid optimization algorithm that integrates Genetic Algorithm

(GA) and Particle Swarm Optimization (PSO). During the initial training phases, GA's extensive global search capabilities guide exploration of the solution space, while in the final stages, PSO's rapid convergence is leveraged to refine and optimize the model parameters. To mitigate overfitting, the dataset is partitioned into training and testing subsets, allocating 80% of the data for training and the remaining 20% for validation. The optimization objective is to minimize the mean squared error (MSE) between the predicted outputs and the corresponding ground truth values.

IX. Design Results and Performance Analysis

The training was carried out on a workstation equipped with 16 GB of RAM and a quad-core Intel processor operating at a maximum clock speed of 2.4 GHz, requiring approximately two minutes to complete.

The training outcomes are depicted in Fig. 5. The final mean squared errors (MSE) for the training and validation datasets were 0.01012 and 0.01804, respectively. Following the completion of the neural network training, the model was employed to generate novel circuit designs. From these, the fifteen top-performing configurations, each optimized for different performance criteria, were selected and summarized in Table III. These configurations are classified into three principal categories based on their optimization objectives: maximization of the DC gain, maximization of the gain-bandwidth product (FoM), and minimization of power consumption. A concise analysis of the salient features for each category is provided in the subsequent subsections.

It should be emphasized that a widely recognized figure of merit, commonly employed in recent and reputable studies for assessing the performance of operational amplifiers [32-35], was computed for each configuration in accordance with (8).

$$FOM = \frac{GBW \times C_{Load}}{p} \tag{8}$$

Also, to evaluate the figure of merit (FOM) of the VCO, this study adopts the standard formulation widely employed in recent oscillator design literature [42-48], as expressed in (9).

$$FoM = L(\nabla\omega) + 10Log\ P_{DC} - 20Log\ (\frac{\omega_0}{\nabla\omega}) \tag{9}$$

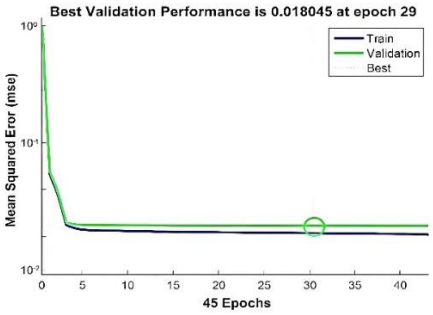

Fig 5. Train and validation error during training

In this formulation, $L\ (\nabla\omega)$ represents the single-sideband phase noise measured at an offset frequency of $\nabla\omega$ while ω_0 denotes the oscillation frequency. The term P_{DC} corresponds to the circuit's power consumption, expressed in mW. Moreover, FTR indicates the frequency tuning range, and ΔV_{tune} specifies the span of the tuning voltage variation.

TABLE III
Performance of Sampled Designs from the Trained ANN

Deign Objective	Low-Frequency Gain (dB)	Gain–Bandwidth Product (FoM) MHz	Power Consumption (mW)	Phase Margin (°)
Objective 1 – Maximum DC Gain	**> 85**	**> 4.0**	**< 1.0**	**Range: 55–100**
Design 1	94.225	4.097	0.05048	58.358
Design 2	92.769	4.036	0.2704	56.351
Design 3	91.85	7.34	0.04575	60.254
Design 4	90.953	5.632	0.1123	73.260
Design 5	89.417	18.01	0.4152	67.523
Objective 2 – Maximum Gain–Bandwidth Product (FoM)	**> 50**	**> 12.0**	**< 1.0**	**Range: 55–100**
Design 6	52.417	52.15	0.764	56.346
Design 7	53.635	32.65	0.9845	61.523
Design 8	55.856	26.78	0.4568	57.369
Design 9	63.658	19.97	0.7348	72.663
Design 10	79.512	18.25	0.6856	57.256
Objective 3 – Minimum Power Consumption	**> 50**	**> 0.1**	**< 0.1**	**Range: 55–100**
Design 11	56.365	0.1231	0.002359	67.236
Design 12	65.472	0.1298	0.003847	68.545
Design 13	58.765	0.4967	0.008153	61.453
Design 14	69.538	0.9573	0.01014	69.547
Design 15	52.142	3.745	0.02878	62.987

The initial five designs were developed with the primary objective of maximizing DC gain while ensuring low power consumption and maintaining sufficient stability, characterized by a high phase margin. Within this subset, Design 1 exhibits the superior overall performance, achieving a gain of 94.225 dB, a power dissipation of merely 0.05048 mW, and a phase margin of 58.36°. Designs 6 through 10 were synthesized to optimize the gain–bandwidth product (Av×GBW). Among these, Design 6 attained the highest figure of merit (FoM) of 52.15. The final cluster, encompassing Designs 11 to 15, was curated to prioritize power consumption minimization. Notably, Design 11 distinguishes itself as one of the most energy-efficient architectures, with a power consumption of only 0.002359 mW, while sustaining acceptable performance metrics such as a gain of 56.365 dB and a phase margin of 67.236°.

The data summarized in Table III substantiate that the neural network model, once trained, can generate a broad spectrum of optimized designs tailored to distinct performance criteria. These designs effectively balance high gain, low power usage, and satisfactory stability, thereby validating the accuracy and practical applicability of the proposed model within the inverse design framework of analog circuits. Corresponding design parameters derived from the neural network predictions—covering transistor channel dimensions, reference current source, compensation capacitance, and load capacitance for maximum low-frequency gain, maximum gain–bandwidth product, and minimum power consumption are detailed in Tables IV, V, and VI, respectively. Furthermore, the frequency response of each group of these designs is presented in Fig.s 6, 7, and 8, respectively. Drawing inspiration from dynamic high fan-in OR gate designs, the proposed neural-network-assisted operational amplifier demonstrates a notable reduction in power consumption while effectively maintaining all critical performance metrics [1].

TABLE IV
The Corresponding Design Parameters of the ANN Predicted Designs to Reach the Best DC Gain.

	$\frac{W_{1,2}}{L_{1,2}}$	$\frac{W_{3,4}}{L_{3,4}}$	$\frac{W_5}{L_5}$	$\frac{W_6}{L_6}$	$\frac{W_7}{L_7}$	$\frac{W_8}{L_8}$	I_{REF} (μA)	C_c (pF)	C_l (pF)
Design 1	17.45 7.536	24.26 22.15	27.63 0.3236	11.23 14.19	0.9852 9.2141	6.745 13.563	14.52	0.1813	2.756
Design 2	28.46 6.423	12.56 5.326	26.41 2.231	2.03 2.043	25.32 25.63	14.55 22.65	53.12	2.023	6.402
Design 3	18.42 11.76	25.36 19.52	29.47 0.2941	11.54 10.362	8.652 25.32	29.45 14.32	7.521	0.0857	1.756
Design 4	22.35 21.54	26.23 30.32	11.74 0.3145	19.44 9.525	5.771 29.47	27.45 13.88	21.632	0.1128	2.145
Design 5	104.56 5.326	30.56 24.68	22.74 0.5123	3.231 24.15	18.54 22.56	18.441 8.023	5.23	0.2223	3.475

TABLE V
Corresponding Design Parameters of the ANN Predicted Designs to Reach the Best Gain-Bandwidth Product.

	$\frac{W_{1,2}}{L_{1,2}}$	$\frac{W_{3,4}}{L_{3,4}}$	$\frac{W_5}{L_5}$	$\frac{W_6}{L_6}$	$\frac{W_7}{L_7}$	$\frac{W_8}{L_8}$	I_{REF} (μA)	C_c (pF)	C_l (pF)
Design 6	40.53 0.5026	87.65 0.2317	9.235 0.355	103.15 3.078	199.41 2.151	5.214 0.8626	78.15	0.0241	8.471
Design 7	22.54 0.5031	15.26 0.3052	77.25 0.2236	7.235 2.066	103.4 3.882	96.24 3.141	34.15	0.7145	9.478
Design 8	47.96 0.5523	37.21 0.3625	84.32 0.2352	68.02 2.145	99.12 3.750	8.512 0.207	17.21	0.6814	5.236
Design 9	39.45 2.231	32.33 1.238	72.78 0.3236	13.56 0.4758	81.54 3.142	48.56 0.702	36.5	1.547	4.214
Design 10	122.45 2.475	76.35 1.215	199.32 0.4452	119.5 2.452	96.47 2.452	165.21 1.315	72.15	2.845	5.745

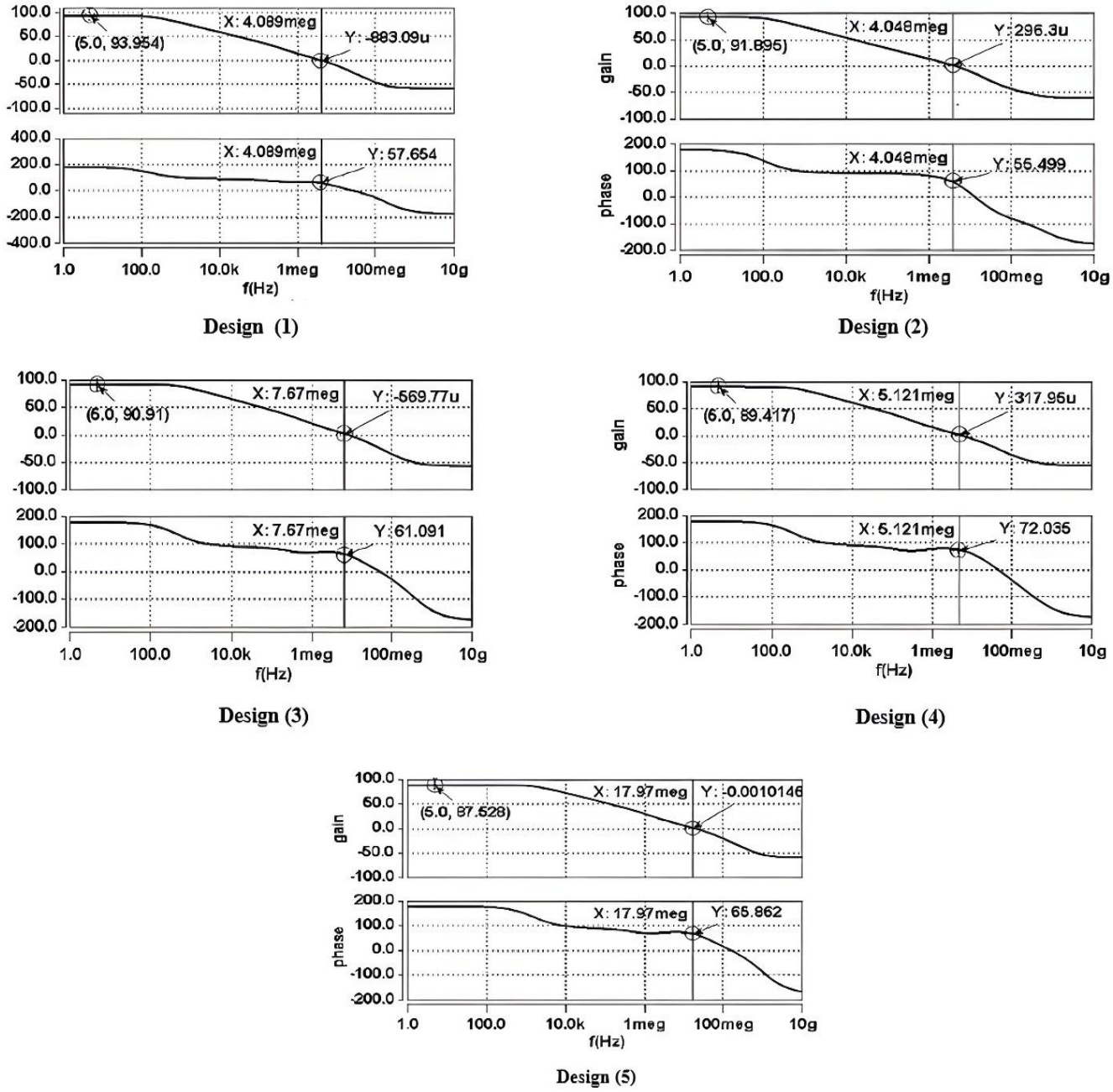

Fig 6. The gain and phase frequency response plots of the predicted designs to reach the best DC gain

TABLE VI
Corresponding Design Parameters of the ANN Predicted Designs to Reach the Best Power Dissipation.

	$W_{1,2}$ $L_{1,2}$	$W_{3,4}$ $L_{3,4}$	W_5 L_5	W_6 L_6	W_7 L_7	W_8 L_8	I_{REF} (μA)	C_c (pF)	C_l (pF)
Design 11	7.452 9.025	17.23 26.74	30.35 0.3625	28.36 14.36	16.78 21.26	28.152 11.25	0.5165	0.5882	6.178
Design 12	9.989 16.53	16.84 14.25	15.89 0.6958	6.36 9.153	8.452 28.51	19.563 10.26	0.5158	1.758	8.541
Design 13	30.26 14.362	11.81 2.365	29.52 0.5685	4.266 6.256	11.53 26.14	19.25 3.845	1.125	2.536	8.658
Design 14	66.23 0.9863	37.23 0.652	1.097 0.4544	76.521 2.712	93.45 2.142	3.891 3.462	1.741	0.00974	9.698
Design 15	22.45 27.65	17.25 25.33	7.032 0.1599	9.256 30.48	4.896 13.48	25.14 29.41	2.475	0.02941	9.075

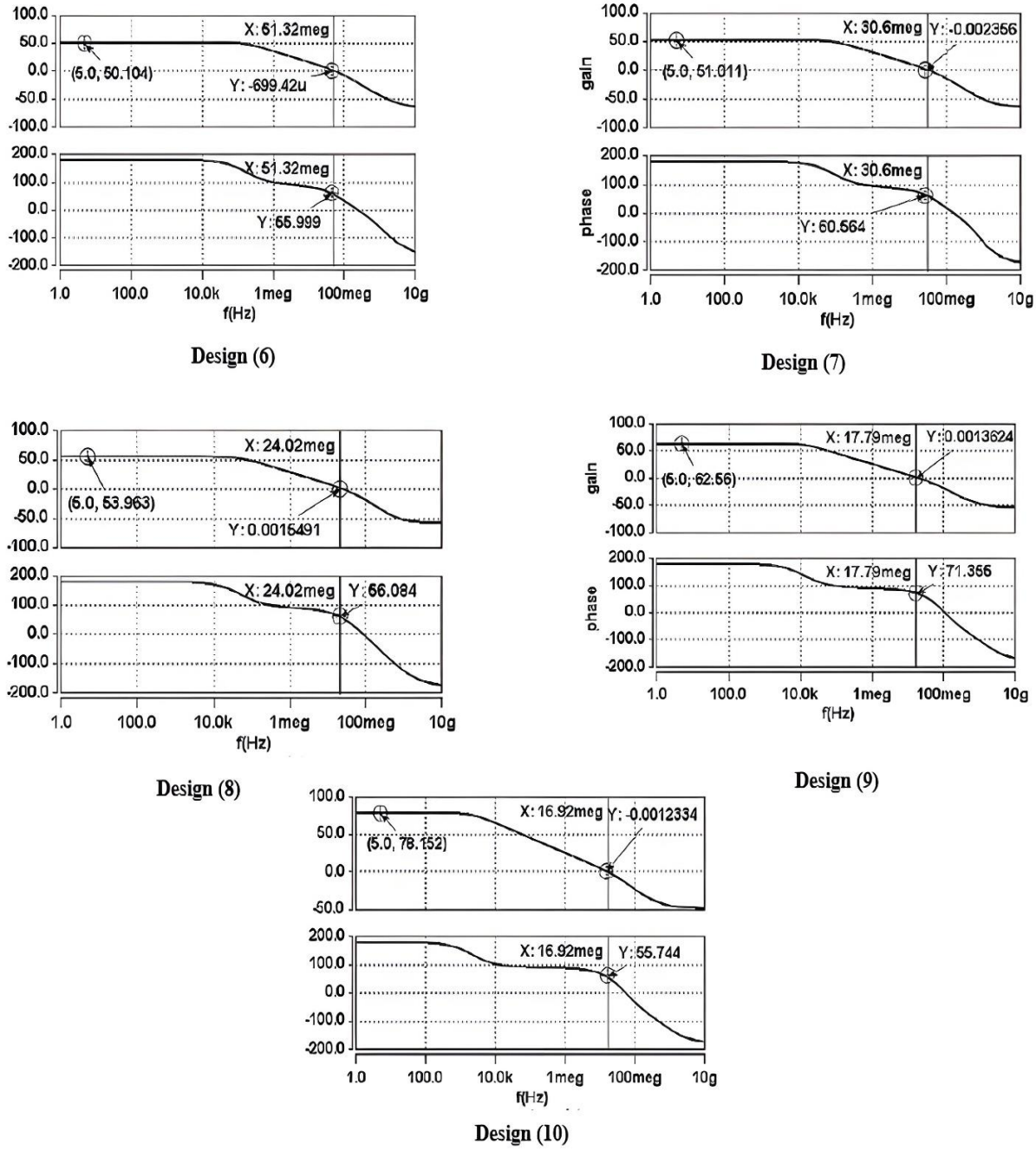

Fig7. The gain and phase frequency response plots of the predicted designs for reaching the best gain-bandwidth product

TABLE VII
Optimized LC-VCO Design Parameters Obtained Using the ANN + GA–PSO Framework

Component	Parameter / Value
Transistors	
M_{1-2}	W/L = 50 / 0.18 $\mu m/\mu m$
M_{3-4}	W/L = 22 / 0.18 $\mu m/\mu m$
M_{5-6}	W/L = 150 / 0.18 $\mu m/\mu m$
Inductor & Capacitors	
L_T	3.25 nH
C_v	184 fF
C_1	1.5 pF
C_2	3 pF

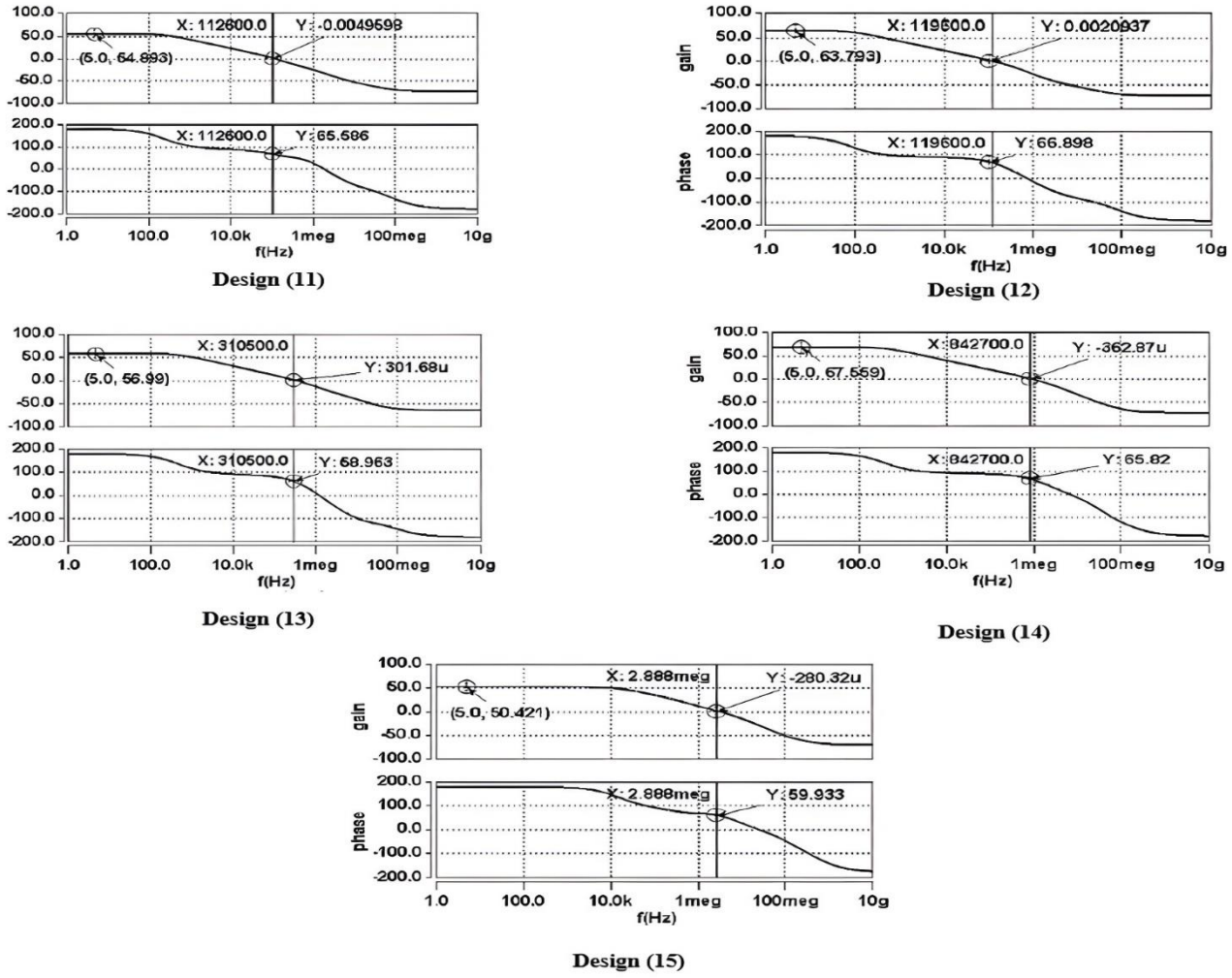

Fig 8. The gain and phase frequency response plots of the predicted designs to reach the best power dissipation

As previously mentioned, to further evaluate the generalization capability of the proposed ANN + GA–PSO framework, a second case study was conducted on a differential CMOS LC voltage-controlled oscillator (LC-VCO) operating at 2.76 GHz in 0.18-µm CMOS technology. The design and simulation of the circuit were carried out using the same ANN + GA–PSO methodology employed in the first case study.

In the LC-VCO design, the key circuit parameters considered as decision variables included the tank capacitors (C1 and C2), transistor dimensions, and voltages. To achieve multi-objective performance optimization, various combinations of these parameters were simulated to obtain the output characteristics of each configuration, including oscillation frequency, power consumption, phase noise, and negative trans conductance. These outputs served as training data for the artificial neural network, allowing the algorithm to determine the optimal parameter combination that ensures reliable startup, low phase noise, and minimal power consumption. In other words, each simulation constituted a training sample for the neural network, enabling it to learn the relationships between circuit parameters and the VCO's final performance, and to propose an optimized configuration. The design parameters of the LC-VCO optimized using the ANN + GA–PSO framework are summarized in Table VII .

As V_{tune} varies from 0 to 1.2 V, the LC-VCO exhibits an oscillation frequency range of 2.68–2.85 GHz. Simulation results demonstrate that, under a 1.4 V supply, the oscillator achieves a frequency of 2.83 GHz, with a power consumption of 864 µW and a phase noise of approximately −118.1 dBc/Hz at a 1 MHz offset. These findings confirm reliable startup, low power consumption, and minimal phase noise, highlighting the capability of the proposed framework to optimize complex analog circuits beyond conventional operational amplifiers. For a more detailed evaluation, the dependencies of oscillation frequency, power consumption, and phase noise on varying control voltages are depicted in Fig. 9.

TABLE VIII
Comparison of Two-Stage Operational Amplifier Design Results with Other Methods

Reference	Amplifier Topology	Technology (µm)	Design Method	Gain–Bandwidth Product (MHz)	Power Consumption (mW)	Load Capacitance (pF)	Figure of Merit (MHz·pF/mW)
[36]	Two-stage with Miller compensation	0.18	Evolutionary Algorithm (MCO)	251	4.2	1	59.761
[37]	Two-stage with Miller compensation and nulling resistor	0.13	Swarm Intelligence-based Algorithm (CRPSO)	111.2	0.01961	0.05	283.528
[38]	Two-stage with Miller compensation	0.35	Hybrid Algorithm (RPSODE)	5.526	0.8794	10	62.838
[39]	Two-stage with Miller compensation	0.13	Metaheuristic Algorithm (WOA)	4.293	0.266	7	112.973
[40]	Two-stage with Miller compensation	0.35	Evolutionary Algorithm (GA)	0.1037	0.0202	0.05	0.256
[40]	Two-stage with Miller compensation	0.35	Swarm Intelligence-based Algorithm (ACO)	0.1	0.01975	0.05	0.253
[41]	Two-stage with Miller compensation	0.18	Metaheuristic Algorithm (GWO)	8.63	1.6	12	64.725
This work	**Two-stage with Miller compensation**	**0.18**	**ANN + GA–PSO (Proposed Method)**	**7.34**	**0.04575**	**0.0857**	**735.23**

TABLE IX
Performance Summary of the Proposed Voltage-Controlled Oscillator (VCO) and some other VCOs

Reference	Tech. (nm)	F_{OSC} (GHz)	V_{DD}(V)	P_{dis} (mW)	TR (%)	PN @1 MHz (dBc/Hz)	FoM
[42]	180	30	1.8	27.4	10.4	106.8	-179
[43]	180	4	1.8	1	NA	-116.8	-188.9
[44]	65	24	1.2	12.8	29	-106	-185
[45]	90	2.6	1	1.875	NA	-120.97	-186.54
[46]	130	2.4	1	0.262	10	-114.7	-188.15
[47]	180	1.7	1.8	37.2	82.4	-110	158.54
[48]	90	1.77	1.2	3.96	6.2	-112	-171
This work	180	2.83	1.4	0.864	6.3	-118.1	-187.5

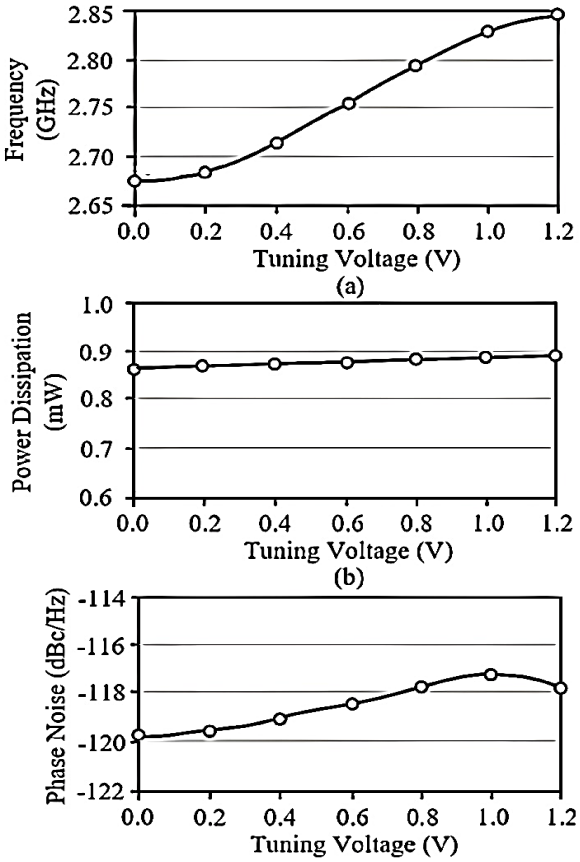

Fig. 9. (a) Output oscillation frequency, (b) power dissipation, and (c) PN of the proposed voltage-controlled oscillator (VCO) for different tuning voltages (Vtune). PN, phase noise.

Furthermore, a comparative overview of the designed VCO using the ANN + HGAPSO hybrid methodology relative to other designs reported in the literature is presented in Table IX.

X. Comparison with Previous Studies and Conclusion

In this study, we introduced a systematic computational intelligence framework for the design and multi-objective optimization of analog integrated circuits, initially validated on a two-stage operational amplifier. The framework synergistically combines Artificial Neural Networks (ANNs) with a hybrid metaheuristic algorithm integrating Genetic Algorithm (GA) and Particle Swarm Optimization (PSO), enabling accurate modeling of the complex relationships between critical design parameters and circuit performance while efficiently navigating the high-dimensional design space. The optimization focused on three primary objectives: maximizing low-frequency gain, improving the gain–bandwidth product, and minimizing power consumption. Among the optimized solutions, the design targeting the gain–bandwidth product (Design 3) achieved a well-balanced trade-off, delivering a gain–bandwidth product of 7.34 MHz, power consumption of 0.046 mW, and a load capacitance of 0.086 pF. Comparative analysis revealed a notable enhancement in the figure of merit (FoM), rising from 283 MHz•pF/mW in previous studies to 735 MHz•pF/mW, representing an approximate 160% improvement.

To further evaluate the generalizability of the proposed approach, the methodology was applied to a differential LC voltage-controlled oscillator (LC-VCO) operating at 2.8 GHz in 0.18-µm CMOS technology. Extensive HSPICE simulations generated comprehensive datasets, enabling the ANN to capture intricate nonlinear dependencies between design variables and performance metrics. The framework successfully predicted optimal device dimensions and biasing conditions, achieving a FoM of 118.1 dBc/Hz for the LC-VCO, comparable to state-of-the-art designs. Overall, the results highlight the robustness, efficiency, and versatility of the ANN-assisted hybrid GA–PSO methodology. This work demonstrates that integrating ANN modeling with hybrid metaheuristic optimization provides a reliable and generalizable strategy for achieving optimal trade-offs in high-performance analog circuits. While the framework is inherently versatile, the current validation primarily relies on the two-stage op-amp and the additional LC-VCO case study. It is also important to acknowledge that additional factors, such as chip area, mismatch effects, process variations, and temperature dependence, play a critical role in analog IC design and can significantly influence the final performance. These aspects are recommended as key directions for future research to further enhance the applicability and comprehensiveness of the proposed framework.

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