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Multi-Stage Active Networks and Switched-Capacitor Synergy: A Novel Ultra-High-Gain DC-DC Converter for EV Powertrains

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***Abstract*- This paper introduces a novel ultra-high-gain DC–DC converter architecture specifically designed for electric vehicle (EV) applications. The converter integrates a switched-capacitor cell with multi-stage inductor–capacitor–two diodes (LC2D) active networks to achieve sequential energy transfer and voltage stacking while maintaining a minimal component count, including only one semiconductor switch. The proposed topology directly addresses the limitations of conventional converters, namely, restricted voltage gains and excessive voltage stress. Simulation results confirm that the converter achieves a voltage gain of up to 10× at a duty cycle of 41.5%, stepping a 45V battery input to a 450V DC bus level typical of EV traction inverters and onboard chargers. The design consistently delivers conversion efficiencies above 95% across a 2-5kW load range, with stable operation, minimal output ripple, and reduced electromagnetic interference. The supported power range aligns with the needs of auxiliary and small-scale EV subsystems. By combining structural simplicity with quantitative performance improvements, the proposed converter offers a compact, reliable, and cost-effective solution for EV powertrains. Overall, the results demonstrate that the converter provides a rigorously validated pathway toward high-gain, high-efficiency DC–DC conversion in EV systems.**

***Index Terms*- DC-DC Converter; Electric Vehicle; Multi-stage Active Networks; Semiconductor Switch; Switched Capacitors.**

I. INTRODUCTION

RECENTLY, the rapid advancement of smart grid infrastructures, electric vehicles (EVs), and renewable energy sources has created a pressing need for power converters that are compact, highly efficient, and capable of delivering elevated voltage levels. Within this context, non-isolated high step-up DC–DC converters (NHSDCs) have become a pivotal solution, as they enable low-voltage energy sources, including batteries, fuel cells, and photovoltaic (PV) modules, to be effectively interfaced with high-voltage DC bus systems. Their transformer-less architecture, reduced cost, and high-power density make them particularly attractive for EV traction systems, onboard chargers, and distributed energy platforms [1, 2]. Unlike isolated converters, NHSDCs eliminate bulky magnetic components and offer simpler control schemes, making them ideal for space-constrained and cost-sensitive applications. However, achieving high voltage gain without compromising efficiency remains a significant challenge. Over the past decade, researchers have proposed a wide variety of topologies to address these issues, focusing on interleaving, soft-switching, bidirectional operation, and modular scalability. Recent literature has introduced a diverse array of NHSDC topologies, each aiming to optimize voltage gain, efficiency, control complexity, and component stress.

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Interleaved structures have gained prominence due to their ability to reduce input current ripple, distribute thermal stress, and improve dynamic response. The converter in [1] employs resonant soft-switching to achieve current auto-balancing in an interleaved configuration, enhancing efficiency and reliability. However, its resonant control demands precise timing and synchronization, increasing implementation complexity and sensitivity to parameter drift. Coupled inductors and switched-capacitor techniques are widely adopted to boost voltage gain without significantly increasing switch count. The topology in [2] achieves high gain with reduced component count, though parasitic effects and layout sensitivity may limit scalability. In [3], voltage multiplier cells and magnetic coupling are used to support renewable applications, but the increased number of passive components raises cost, volume, and electromagnetic interference (EMI) concerns. The converter in [4] balances gain and stress effectively using a coupled-inductor-based structure, yet its performance under dynamic load conditions and partial shading scenarios remains underexplored.

Modular and expandable designs offer flexibility for multi-source and multi-load systems. The topology in [5] supports low switching stress and scalability, making it suitable for PV-based microgrids. However, it lacks built-in fault-tolerant mechanisms, which are critical for safety in automotive environments. The ultrahigh step-up converter in [6] delivers impressive voltage gain with minimal input ripple, though its elevated duty cycle may degrade transient response and increase conduction losses. Improved magnetic energy harnessing is presented in [7], where optimized interleaving enhances energy transfer efficiency. Nevertheless, its phase balancing control adds complexity and may require digital implementation. Bidirectional energy flow is essential in EVs, where power must flow both from the battery to the motor and from regenerative braking back to the battery. This is addressed in [8], which introduces a non-isolated interleaved bidirectional converter with minimal switch count. While efficient in both directions, its reverse-mode performance is slightly inferior, and its control strategy requires careful tuning to avoid shoot-through faults. Soft-switching is further explored in [9], where Dickson switched-capacitor cells are integrated with interleaving to enable zero voltage switching (ZVS), reducing switching losses and thermal stress. However, the converter’s high-frequency operation may exacerbate EMI and necessitate advanced filtering.

Advanced cell configurations continue to evolve. The converter in [10] employs modified active switched-inductor and switched-capacitor cells to achieve high gain while minimizing voltage stress across semiconductors. Yet, its control loop stability under varying load conditions is not fully validated. Resonant techniques in [11] enable wide load adaptability and soft-switching benefits, but require careful tuning of the resonant tank and may suffer from reduced efficiency under light load. The 2-MHz hybrid converter in [12] achieves ZVS and compactness, though its high switching frequency demands advanced thermal management and EMI shielding, which may increase system cost. Control flexibility is expanded in [13] through quasi-Z-source converters with negative output characteristics, offering enhanced fault tolerance and dynamic adaptability. However, their negative voltage behavior complicates integration with standard loads. Grid-tied applications benefit from [14], which integrates a soft-switched boost-flyback converter for solar PV systems. While effective, its transformer design introduces leakage inductance and requires snubber circuits to suppress voltage spikes. Voltage stress reduction is emphasized in [15], where a single-core ZVS configuration is used to lower stress on switches while maintaining high gain. While effective, its three-level structure increases control complexity and may require additional gate drivers. A notable contribution comes in [16], where a modular high-gain converter architecture is proposed, integrating switched-capacitor and coupled-inductor techniques. The design achieves over 94% efficiency across a wide duty cycle range and emphasizes layout optimization, gate drive simplicity, and reduced voltage stress. Its modularity and experimental validation under realistic operating conditions make it highly suitable for EV applications. However, thermal management at higher power levels and partial-load behavior remain areas for further investigation. The quasi-Z-source design in [17] enhances gain and efficiency through coupled inductors, but its startup behavior under low input voltage is not addressed, which may affect cold-start reliability. Bidirectional converters with zero ripple current, such as [18], improve energy stability and battery lifespan, though their control requires high-speed current sensing and precise timing. Multi-mode operation is explored in [19], which presents a triple-switch converter capable of adapting to varying load conditions and operating modes. While this enhances versatility, the triple-switch configuration increases gate drive complexity and may reduce overall efficiency under partial loads. Transformer-based voltage multiplier cells are revisited in [20], combining dual boost stages for enhanced gain and a compact layout. However, their magnetic coupling demands precise winding ratios and careful PCB layout to avoid flux imbalance. The converter in [21] uses cente tapped inductors to achieve high conversion ratios with reduced component count, though its magnetic core design may limit miniaturization and thermal dissipation. Recent contributions from 2024–2025 further enrich the landscape and reflect the field’s ongoing momentum. The converter in [22] integrates voltage-lift capacitors and multiplier cells in an interleaved structure, achieving high gain with reduced switch stress. Its modularity and low component count make it attractive for compact EV powertrains. However, its performance under partial load conditions and EMI behavior requires further investigation. In [23], a novel soft-switched trans-inverse converter is proposed, offering ultra-high voltage gain with ZVS operation. This topology significantly reduces switching losses and improves thermal efficiency, particularly in high-frequency EV applications. Nonetheless, the converter’s control loop is sensitive to parameter variations, necessitating robust digital control strategies.

Bidirectional energy flow is further enhanced in [24], which presents a wide-gain converter based on switched inductors for EV battery systems. Its dual-mode operation supports both charging and propulsion, with low input current ripple and high efficiency. The main drawback lies in its increased gate drive complexity. Researchers in [25] propose a cost-effective and modular step-up converter tailored for EV applications; however, its scalability to higher power levels remains limited due to thermal constraints and magnetic core saturation.

Additional contributions [26]-[32] further expand the design space and offer alternative approaches to high-gain DC–DC conversion. The topology in [26] employs a switched-voltage multiplier cell combined with resonant operation to achieve high step-up ratios with reduced switching losses. The converter in [27] utilizes a quadratic flying-capacitor configuration to enhance voltage gain with minimal switch count. In [28], voltage multiplier cells are integrated into a quadratic boost framework, enabling scalable gain and modular expansion. A SEPIC-based converter without coupled inductors is proposed in [29], targeting PV systems. Its simplified magnetic structure reduces core saturation risk and improves manufacturability, though its efficiency under dynamic load conditions remains moderate. For fuel cell vehicle applications, [30] presents a wide-input-range boost converter capable of maintaining stable operation across varying voltages. Despite its robustness, the elevated duty cycle introduces conduction losses and may degrade transient response. Transformer-less topologies continue to gain traction, with [31] eliminating magnetic coupling entirely to reduce cost and volume. While promising for compact systems, the absence of fault-tolerant mechanisms and limited experimental validation restricts its deployment in safety-critical environments. Finally, [32] introduces a multi-stage converter using an active network, demonstrating low switch stress. Its modularity and efficiency are notable, though scalability to higher power levels introduces control coordination challenges.

In summary, the selected literature [1]-[32] reflects a comprehensive evolution of NHSDC architectures, from interleaved and soft-switched designs to bidirectional and modular topologies. Each converter offers distinct advantages; however, persistent challenges remain. This paper builds upon these insights to propose a robust modelling and performance enhancement framework for DC–DC converters tailored to the stringent requirements of EV applications. So, this work presents a novel high step-up DC–DC converter, featuring switched capacitors and multi-stage active networks while utilizing a minimal component count, including just one semiconductor switch. The design directly addresses the long-standing limitations of conventional converters, namely restricted voltage gains and excessive voltage stress, which often compromise efficiency and reliability. By merging structural simplicity with superior performance, the proposed topology marks a meaningful advancement in converter technology, offering a compact and cost-effective solution for systems where efficiency and robustness are critical. The development process followed a rigorous methodology, combining theoretical modelling with simulation-based validation to ensure that both operating principles and performance characteristics were thoroughly assessed. Central to the design is the strategic use of switched capacitors to achieve high voltage gains without resorting to complex circuitry or multiple active switches, thereby reducing control overhead, manufacturing cost, and potential reliability concerns. Simulation results highlight the converter’s ability to deliver significant improvements in voltage gain while simultaneously alleviating voltage stress across components, leading to higher efficiency and lower EMI compared to traditional boost converters. The findings further confirm stable operation under diverse load conditions, with low output ripple and consistently high conversion efficiency, thereby validating the theoretical predictions and underscoring the practical viability of the proposed architecture.

Accordingly, the innovative aspects of the present study can be summarized as follows:

- A converter built with the fewest possible parts, including only one semiconductor switch.
- Strategic use of switched capacitors to achieve high voltage gain without complex circuitry.
- A specific multi-stage active network was introduced in our manuscript, composed of an L–C–two-diode (LC2D) cell. Each LC2D cell integrates one inductor (L), one capacitor (C), and two diodes (2D), arranged in a manner that enables sequential energy transfer and voltage stacking across multiple stages.
- Significant improvement in output voltage compared to conventional step-up converters.
- Lower stress across components, improving reliability and extending device lifespan.
- Consistent performance with low ripple and high efficiency across different load conditions.

The remainder of this paper is structured as follows: Section II introduces the topology of the proposed converter, emphasizing its configuration and operating principles. Sections III and IV present the steady-state analysis, including the derivation of voltage-gain equations and the assessment of voltage stresses across the components. Sections V and VI provide a comparative study with conventional converters and efficiency analysis, highlighting the proposed design’s advantages. Section VII reports the simulation results, which validate the theoretical analysis. Finally, Section VIII concludes by summarizing the main contributions and suggesting future research directions in EV power systems.

II. PROPOSED HIGH STEP-UP DC-DC CONVERTER

This section introduces a novel high-gain DC-DC boost converter topology, tailored for EV applications. The proposed design is based on current-source switching converters and incorporates switched capacitors along with multi-stage active LC2D networks, as illustrated in Fig. 1.

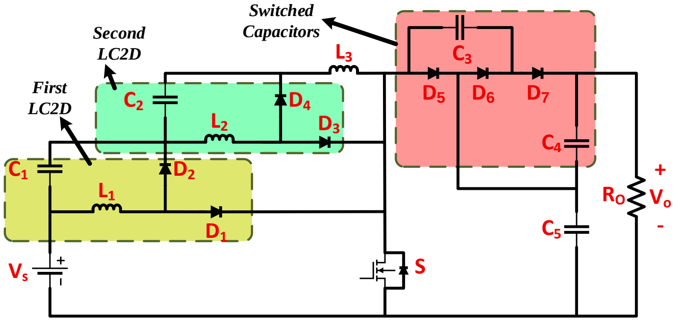
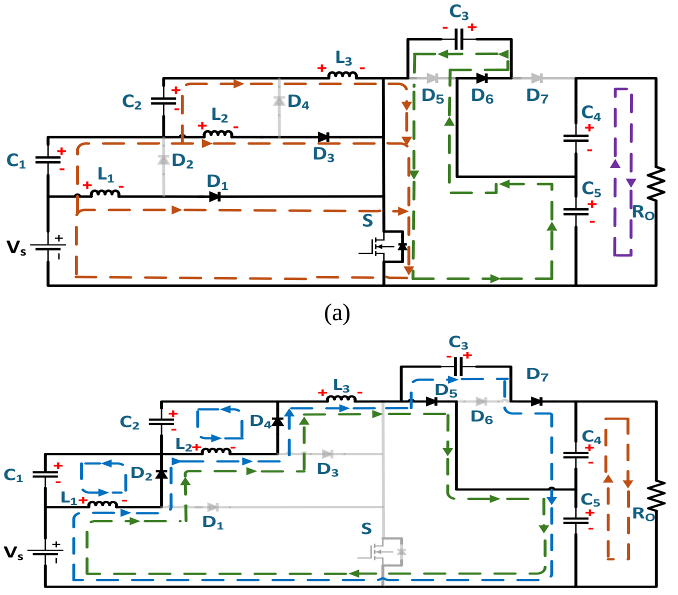


Fig. 1. Proposed high step-up DC-DC converter based on application in EVs using switched capacitors and multi-stage active LC2D networks.

The proposed converter offers several notable benefits: it achieves exceptionally high voltage amplification, maintains a positive output polarity, and significantly reduces voltage stress on the switching device. By relying on standard components, parasitic effects are minimized, while the use of a single semiconductor switch and a streamlined design with few elements ensures compactness and high overall efficiency. Structurally, the converter consists of 16 components in total: three inductors, five capacitors, seven diodes, and one switching device. On the left side of the circuit, multi-stage active networks are constructed using two-cell LC2D units. Within each LC2D cell, energy stored in one inductor is first transferred to a capacitor. The capacitor, in conjunction with the input source, transfers energy to a subsequent inductor. The energy accumulated in both inductors is then released to the load, and this process is continuously repeated across all LC2D stages. Also, a switched-capacitor arrangement is employed. This design supports cascading, modularity, and seamless integration, all of which contribute to achieving ultra-high voltage gain across multiple levels. The converter functions in two distinct operating states: (I) when the switch is ON and (II) when the switch is OFF. These modes are depicted in Fig. 2.



(a)

(b)

Fig. 2. Operating modes of the proposed high step-up DC-DC converter, utilizing switched capacitors and multi-stage active LC2D networks. (a) Mode I, and (b) Mode II.

III. OPERATING MODES OF THE PROPOSED CONVERTER

To facilitate the steady-state analysis of the proposed converter, several simplifying assumptions are adopted. All inductors and capacitors are assumed to be sufficiently large so that their voltage and current ripples can be neglected. The switching elements, namely the diode and the power switch, are considered ideal, with no forward voltage drop or switching losses. Under these conditions, the converter operates in two distinct modes corresponding to the ON and OFF states of the switch. The circuit configurations for both operating modes are depicted in Fig. 2, while the principal voltage and current waveforms are shown in Fig. 3.

A. *Mode I [$t_0 < t < t_1$]*

As depicted in Fig. 3, at time T_0 the switch is turned ON. This action forces diodes D_2, D_4, D_5, and D_7 into a reverse-biased state, while the inductors begin charging. Specifically, inductor L_1 is energized directly by the input source V_S, whereas inductor L_2 is charged through the combined contribution of the input source and the capacitor C_1 $(V_S + V_{C1})$. In addition, as shown in Fig. 2(a), the inductor L_3 is charged by the input source together with capacitors C_1 and C_2 $(V_S + V_{C1} + V_{C2})$. Under steady-state operation, the capacitor voltages satisfy the relations $V_{C1} = V_S D/(1-D)$ and $V_{C2} = V_S D/(1-D)^2$, which are obtained by applying the volt-second balance principle to inductors L_1 and L_2.

The voltages across L_1, L_2 and L_3 are calculated using Kirchhoff's voltage law (KVL), by substituting V_{C1} and V_{C2} into the multi-stage section of the converter:

$$VL_1 = V_s \tag{1}$$

$$VL_2 = \frac{V_s}{1-D} \tag{2}$$

$$VL_3 = \frac{V_s}{(1-D)^2} \tag{3}$$

Capacitors C_3 and C_5 are equal to each other according to the current loop in Fig. 2(a):

$$VC_3 = VC_5 \tag{4}$$

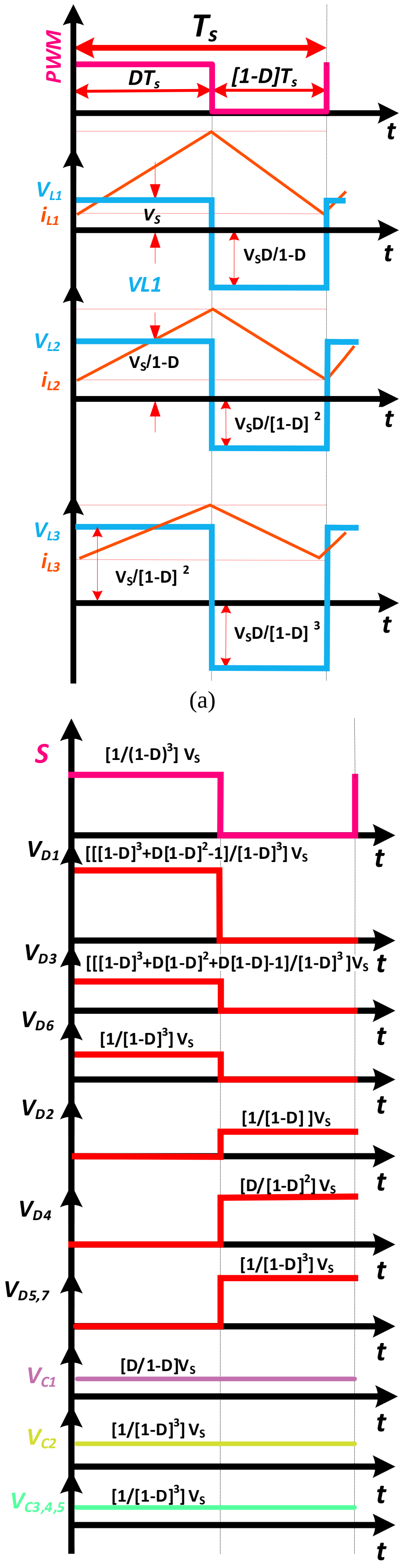
Finally, the series capacitors (C_4 and C_5) transfer energy to the load:

$$V_o = VC_4 + VC_5 \tag{5}$$

B. *Mode II [$t_1 < t < t_2$]:*

As shown in Fig. 2(b), the switch turns OFF and diodes D_1, D_3 and D_6 become reverse biased; also, five current loops appear in the circuit. Inductor L_1 transfers its stored energy to capacitor C_1:

$$VL_1 = VC_1 = \frac{V_s D}{(1-D)} \tag{6}$$



(a)

(b)

Fig. 3. Voltage and current waveforms of converter elements; (a) PWM signal and Inductors; (b) Diodes and the power switch.

Inductor L_2 transfers its stored energy to capacitor C_2, thereby charging it during the switch-off interval. This energy transfer occurs as part of one of the five current loops that emerge in the circuit when diode D_4 is forward-biased, as illustrated in Fig. 2(b). The charging process of C_2 contributes to the voltage boosting mechanism of the converter and plays a key role in the multi-stage energy accumulation strategy employed in the LC2D network:

$$VL_2 = VC_2 = \frac{V_s D}{(1-D)^2} \tag{7}$$

The voltage equations corresponding to the aforementioned current loops can be formulated as follows. Each loop represents a distinct energy transfer path during the switch-off interval, involving specific combinations of inductors, capacitors, and diodes. By applying KVL to each loop and incorporating the steady-state capacitor voltages derived earlier, the voltage relationships within the multi-stage section of the converter can be systematically expressed. These equations provide insight into the internal dynamics of the converter and serve as the foundation for analysing its voltage gain and operational behaviour:

$$VL_3 = V_S - V_o + VC_1 + VC_2 + VC_3 \tag{8}$$

The input voltage source V_s, together with the inductors L_1, L_2 and L_3, charges capacitor C_5 through the diodes D_2, D_4 and D_5. This energy transfer occurs during the switch-off interval, forming one of the key current loops responsible for boosting the output voltage. The combined contribution of the input source and the energy stored in the inductors enables capacitor C_5 to reach a higher voltage level, which plays a crucial role in the overall voltage gain of the converter. This mechanism is essential to the multi-stage architecture and highlights the coordinated operation of the LC2D network and the switched-capacitor structure:

$$VC_5 = V_s - VL_1 - VL_2 - VL_3 \tag{9}$$

The input voltage source Vs, along with inductors L_1, L_2, and L_3, as well as capacitor C_3, charges the series-connected capacitors C_4 and C_5 through diodes D_2, D_4 and D_7. This energy transfer path plays a critical role in elevating the voltage level across the output stage and contributes to the overall gain of the converter during the switch-off interval:

$$V_o = V_s - VL_1 - VL_2 - VL_3 - VC_3 \tag{10}$$

C_3 and C_4 also exhibit equal voltage levels in this mode, as dictated by the corresponding current loop. This equality results from their symmetrical placement and identical charging paths during the energy transfer process, as stated in (11).

$$V_{C_3} = V_{C_4} \tag{11}$$

The series-connected capacitors C_4 and C_5 continue to deliver energy to the load during this interval. This sustained energy transfer ensures a stable output voltage and contributes to the high voltage gain characteristic of the converter's architecture:

$$V_o = V_{C_4} + V_{C_5} \tag{12}$$

Based on the operating principles discussed for both converter modes, the voltages across the capacitors are to be linear and constant. Therefore, the following relationships hold true:

$$V_{C_3} = V_{C_4} = V_{C_5} \tag{13}$$

According to equations (12) and (5) and considering equation (13) between the output capacitors and capacitor C_3, the following equation is derived as (14).

$$V_{C_4} = V_{C_5} = \frac{V_o}{2} = V_{C_3} \tag{14}$$

As stated by the volt-second balance principle, the average voltage across inductor L_3 over one switching period Ts is zero. This condition allows us to equate the areas under the voltage-time curve during the ON and OFF intervals of the switch. By applying this principle to L_3 and substituting the relevant capacitor voltages and diode conduction states, we can derive a key relationship that contributes to the overall voltage gain expression of the converter:

$$\langle VL_3 \rangle = \frac{VL_{3,Mode\ I} * DT + VL_{3,Mode\ II} * (1-D)T}{T} \tag{15}$$

Also, according to equation (14), the value of capacitor C_3 can be set as follows:

$$V_{C_3} = \frac{V_o}{2} \tag{16}$$

The voltage gain of the proposed converter is derived based on the analytical relationships presented in equations (1) through (16), which encompass both switching modes and the behaviour of inductors, capacitors, and diodes throughout the operation cycle. These equations collectively describe the energy transfer mechanisms, voltage stacking effects, and the role of switched-capacitor and multi-stage active networks in boosting the output voltage. Accordingly, the DC voltage gain of the proposed converter is explicitly expressed in equation (17), which serves as the final formulation capturing the converter's performance under steady-state conditions:

$$Gain\ (G) = \frac{V_o}{V_s} = \frac{2}{(1-D)^3} \tag{17}$$

IV. VOLTAGE STRESSES ACROSS COMPONENTS

To properly design the circuit components, it is essential to determine the voltage stress across each element, including capacitors, diodes, and the power switch. This section presents the voltage stresses of the capacitors VC_1, VC_2, VC_3, VC_4, and VC_5, based on the analytical expressions derived in equations (6), (7), (11), (13) and (14).
The voltage stress across capacitor C_1 can be obtained as follows:

$$VC_1^{srtees} = \left(\frac{D}{1-D}\right)V_s \tag{18}$$

The voltage across capacitor C_2 can also be obtained as follows:

$$VC_2^{strees} = \left(\frac{D}{(1-D)^2}\right)V_s \tag{19}$$

According to equations (11), (12), and (13), and considering linear and constant capacitor voltages, capacitors C_3, C_4 and C_5 exhibit equal voltage levels due to their identical current loop behaviour. Therefore, the voltage stress across these capacitors can be calculated as follows:

$$\begin{aligned} VC_3^{strees} &= VC_4^{strees} = VC_5^{strees} \\ &= \left(\frac{1}{(1-D)^3}\right)V_s \end{aligned} \tag{20}$$

The voltage stress across the diodes is defined during their reverse-biased state, meaning that the voltage across each diode is considered zero when it is conducting. The voltage stresses of diodes D_2, D_4, D_5 and D_7 in the OFF state (Mode I) are determined by the voltages of the associated capacitors. Therefore, their voltage stresses can be calculated accordingly. By applying KVL to the current loop indicated in Fig. 2(a) and based on equations (1) and (6), the voltage stress across diode D_2 can be derived.
Thus, the voltage stress of diode D_2 is given by:

$$VD_2^{strees} = \left(\frac{1}{1-D}\right)V_s \tag{21}$$

Similarly, by applying KVL to the current loop indicated in Fig. 2(a), and based on equations (2) and (7), the voltage stress across diode D_4 can be determined:

$$VD_4^{strees} = \left(\frac{1}{(1-D)^2}\right)V_s \tag{22}$$

By applying KVL to the current loop involving diode D_5, as illustrated in Fig. 2(a), and referring to equation (14), it is observed that the voltage across D_5 corresponds to the voltage of capacitor C_3.

$$VD_5^{strees} = \left(\frac{1}{(1-D)^3}\right) V_s \tag{23}$$

Diode D_7 is also directly associated with capacitor C_4, and its voltage stress corresponds to the voltage across this capacitor. Based on equations (14) and (20), the voltage stress of diode D_7 can be determined as follows:

$$VD_7^{strees} = \left(\frac{1}{(1-D)^3}\right) V_s \tag{24}$$

The voltage stresses of diodes D_1, D_3, and D_6 during their OFF state (Mode II) are determined by the voltages of the associated capacitors. By applying KVL to the loop indicated in Fig. 2(b), and referring to equations (6) and (14), the voltage stress across diode D_1 can be derived. Accordingly, the voltage stress of diode D_1 is calculated as follows:

$$VD_1^{strees} = \left(\frac{(1-D)^3 + D(1-D)^2 - 1}{(1-D)^3}\right) V_s \tag{25}$$

Similarly, by applying KVL to the current loop indicated in Fig. 2(b) and referring to equations (6), (7), and (14), the voltage stress across diode D_3 can be determined. Accordingly, the voltage stress of diode D_3 is calculated as follows:

$$VD_3^{strees} = \left(\frac{(1-D)^3 + D(1-D)^2 + D(1-D) - 1}{(1-D)^3}\right) V_s \tag{26}$$

The current loop involving diode D_6, as illustrated in Fig. 2(b), and based on equation (14), it is evident that the voltage across D_6 corresponds to the voltage of capacitor C_3. Therefore, by referring to equation (20), the voltage stress of diode D_6 is determined as:

$$VD_6^{strees} = \left(\frac{1}{(1-D)^3}\right) V_s \tag{27}$$

The voltage stress imposed on the power MOSFET can be derived by applying KVL to the loop highlighted in Fig. 2(b). It should be emphasized that this stress is assessed during the OFF state of the switch, since the voltage across it is assumed to be zero while conducting. Consequently, considering the circuit topology and the formulation presented in equation (14), the voltage stress across switch S can be expressed as:

$$V_{MOSFET}^{strees} = \left(\frac{1}{(1-D)^3}\right) V_s \tag{28}$$

The voltage stresses of the components in the proposed converter are determined based on the analytical expressions derived in equations (18) through (28). These expressions comprehensively describe the voltage behavior of all key elements, including capacitors, diodes, and the power switch, under their respective OFF-state conditions. This analysis is critical for proper component selection, ensuring reliable operation, and preventing premature failure due to overvoltage. Voltage stress directly influences the breakdown voltage rating, thermal performance, and long-term durability of each component. Therefore, accurate estimation during the design phase is essential not only for electrical safety but also for cost optimization and system robustness. The derived expressions reflect the converter's steady-state behavior and are based on ideal assumptions such as continuous conduction mode (CCM), negligible parasitic effects, and ideal switching transitions. While these assumptions simplify the analysis, they provide a reliable baseline for initial component selection and layout planning. To enhance clarity and streamline the design process, Table I summarizes the voltage stresses of all components in a structured format. The table is organized by component type, grouping capacitors, diodes, and switches, and sorted according to their respective voltage stress levels. This allows designers to quickly identify the maximum voltage each element must withstand and select appropriate commercial components with sufficient safety margins.

For instance, capacitors subjected to high voltage stress may require film or ceramic types with high dielectric strength, while diodes must be chosen based on reverse recovery characteristics and peak inverse voltage ratings. Moreover, understanding voltage stress distribution helps in optimizing PCB layout, minimizing (EMI), and improving thermal dissipation. Components with higher voltage stress often demand greater spacing, shielding, or snubber circuits to suppress voltage spikes and ringing. In high-frequency applications, such as EV powertrains, even small mismatches in voltage stress can lead to significant reliability issues over time. Although the current analysis is based on ideal conditions, it forms the foundation for further refinement through simulation and experimental validation. In future work, parasitic elements such as stray inductance, junction capacitance, and switching losses will be incorporated to evaluate dynamic voltage stress under real-world operating scenarios. This multi-stage approach ensures that the converter design remains robust, scalable, and compliant with industry standards.

TABLE I

Design Considerations (Voltage Stresses) for Capacitors, Diodes, Switch and Related Parameters

Components	*Voltage stresses across Components*
$\boldsymbol{C_1}$	$\left(\frac{D}{1-D}\right) V_s$
$\boldsymbol{C_2}$	$\left(\frac{D}{(1-D)^2}\right) V_s$
$\boldsymbol{C_3, C_4, C_5}$	$\left(\frac{1}{(1-D)^3}\right) V_s$
$\boldsymbol{D_1}$	$\left(\frac{(1-D)^3 + D(1-D)^2 - 1}{(1-D)^3}\right) V_s$
$\boldsymbol{D_2}$	$\left(\frac{1}{1-D}\right) V_s$
$\boldsymbol{D_3}$	$\left(\frac{(1-D)^3 + D(1-D)^2 + D(1-D) - 1}{(1-D)^3}\right) V_s$
$\boldsymbol{D_4}$	$\left(\frac{1}{(1-D)^2}\right) V_s$

Components	*Voltage stresses across Components*
D_5	$\left(\frac{1}{(1-D)^3}\right)V_s$
D_6	$\left(\frac{1}{(1-D)^3}\right)V_s$
D_7	$\left(\frac{1}{(1-D)^3}\right)V_s$
S	$\left(\frac{1}{(1-D)^3}\right)V_s$

TABLE II

Comparing the Performance of Similar Converters with the Proposed Converter

Topology	**[26]**	**[27]**	**[28]**	**[29]**	**[30]**	**[31]**	**[32]**	**Proposed**
Switches Count	4	2	1	2	2	2	1	1
Diodes Count	12	4	4	3	5	5	5	7
Capacitors Count	12	3	4	4	5	6	3	5
Inductors Count	4	2	3	3	2	3	3	3
Maximum Gain at D = 0.8	60	50	45	49	95	70	125	250
Voltage Gain	$\frac{12}{(1-D)}$	$\frac{2}{(1-D)^2}$	$\frac{1+D}{(1-D)^2}$	$\frac{D^2+2D+1}{(1-D)^2}$	$\frac{(3+D)}{(1-D)^2}$	$\frac{(2+D)}{(1-D)^2}$	$\frac{1}{(1-D)^3}$	$\frac{2}{(1-D)^3}$
Maximum Voltage Stress on the switches	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{2+D}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^3}$	$\frac{V_{in}}{(1-D)^3}$
Maximum Voltage Stress on the Diodes	$\frac{2V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{2-D}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{2+D}{(1-D)^2}V_{in}$	$\frac{V_{in}}{2(1-D)^3}$	$\frac{V_{in}}{(1-D)^3}$
Power Density	Small	Small	Medium	Medium	Medium	Medium	High	High
Maximum Eff.%	93%	92%	88%	91%	93.5%	95.22%	94%	95.5%

V. COMPARISON STUDY

Table II provides a comparative assessment of conventional converter topologies, highlighting key parameters such as output voltage gain, the number of semiconductor devices, and reactive components. As indicated, the proposed design achieves a DC voltage gain greater than 80 at a duty cycle of 70%, while requiring only 12 components in total, including a single active semiconductor switch. Within this architecture, the capacitors play a crucial role by storing energy in the high-voltage inductors. The stored energy is then transferred to the right-hand section of the circuit, where a switched-capacitor network is integrated. This arrangement enables efficient energy delivery and supports the attainment of ultra-high voltage gain. Notably, the involvement of capacitors in the discharge path influences the output voltage, primarily due to the parasitic elements inherent in the capacitor structure.

As shown in Table II and Fig. 4, a comparative study has been carried out between the proposed converter and several existing topologies, with particular attention to output voltage gain, overall component count, maximum voltage stress on the switches, maximum voltage stress on the diodes, power density, and efficiency. From Fig. 4(a), among the reported designs, the converter in [32] delivers a comparatively high voltage gain, whereas the topology described in [28] demonstrates the weakest performance under equivalent operating conditions. In contrast, the proposed converter achieves the highest DC voltage gain of all the structures examined, underscoring its superior efficiency and optimized design. Converter [27], although composed of only 11 components, delivers limited voltage gain and relies on two active semiconductor switches. This dual-switch configuration increases control complexity and necessitates additional gate driver circuitry, which can impact system cost and reliability. In contrast, the proposed converter achieves significantly higher gain using just one active switch, simplifying the control strategy and reducing the number of required auxiliary circuits. Converter [30] achieves notable voltage amplification at duty cycles below 74%, but it incorporates 14 components, including two semiconductor switches. While its performance is commendable, the increased component count and control overhead make it less favorable for compact and cost-sensitive applications. The proposed converter, by comparison, maintains high voltage gain with only 12 components and a single switch, offering a more efficient and scalable solution. Although the topology in [32] achieves high gain, it includes 32 components, among them four active switches, which substantially increase control complexity, power loss, and layout constraints.

Moreover, parasitic elements within its active capacitor network contribute to a noticeable reduction in effective voltage gain, especially at duty cycles below 71%. Overall, the proposed converter demonstrates a remarkable balance between performance and simplicity. Its ability to achieve a DC voltage gain exceeding 250 at an 80% duty cycle, using minimal components and a single switch, sets it apart from conventional designs. This not only reduces implementation cost and control burden but also enhances reliability and integration potential for EV and renewable energy applications.

The topology presented in [29] introduces a modular high-gain converter architecture that integrates switched-capacitor cells and coupled inductors. It achieves over 94% efficiency across a wide duty cycle range and emphasizes layout optimization, gate drive simplicity, and reduced voltage stress. Its modularity and experimental validation under realistic operating conditions make it highly suitable for EV applications. In contrast, the proposed converter in this work achieves a DC voltage gain exceeding 250 at a duty cycle of 80%, using only 12 components, including a single semiconductor switch. This minimalist design significantly reduces control complexity, gate driver requirements, and overall implementation cost. While [29] topology relies on multiple coupled inductors and a more distributed energy transfer mechanism, the proposed converter utilizes high-voltage inductors and switched-capacitor networks to concentrate energy delivery with fewer stages. From a voltage stress perspective, both converters aim to minimize peak voltages across switching devices. However, the proposed design achieves this with fewer components and a simpler discharge path, whereas [26] topology requires careful magnetic coupling and layout symmetry to maintain voltage balance. In terms of scalability, the [29] converter offers modular expansion, making it suitable for multi-source systems. The proposed converter, while less modular, achieves comparable or superior gain with a more compact structure, making it ideal for space-constrained EV platforms. Overall, the proposed converter demonstrates a more aggressive gain-to-complexity ratio, achieving high performance with minimal hardware, while [26] topology offers broader flexibility and proven experimental robustness.

Fig. 4(b) and (c) present a normalized comparison of semiconductor voltage stresses across seven high-step-up converter topologies, evaluated at a standardized voltage gain of 5x ($V_o/V_{in} = 5$). This normalization enables a fair performance assessment by compensating for intrinsic topological differences.

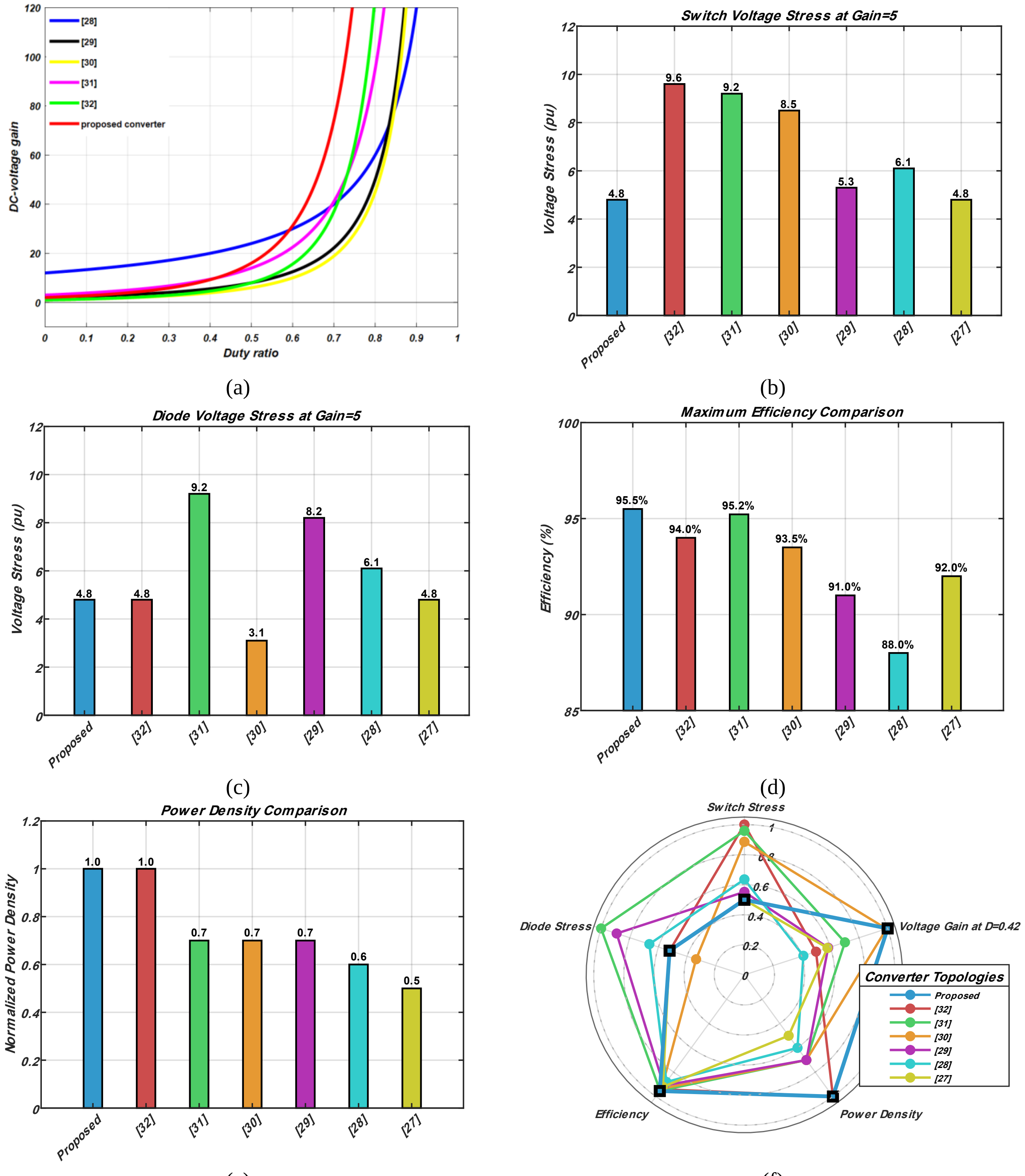
As shown in Fig. 4(a), the proposed converter exhibits the lowest switch voltage stress (4.8 pu), representing a 50% reduction compared to converters [32] and [31], which endure approximately 9.6 pu and 9.2 pu, respectively. This substantial reduction directly translates to lower switching losses, reduced EMI, and the ability to employ lower-voltage-rated (and thus lower-cost) MOSFETs. While Fig. 4(b) indicates that converter [30] achieves a marginally lower diode stress (3.1 pu versus 4.8 pu for the proposed design), this advantage is offset by its significantly higher switch stress (8.5 pu) and inferior efficiency profile, as will be demonstrated. The proposed topology's balanced stress distribution, coupled with its minimal component count, validates its design efficiency, where a minor compromise in diode stress is strategically exchanged for major gains in switch performance, overall efficiency, and system-level cost-effectiveness, making it particularly advantageous for EV power systems.

The efficiency and power density benchmarking in Fig. 4(d) and (e) reveal the proposed converter's exceptional performance in terms of energy conversion quality and compactness. Fig. 4(d) demonstrates that the proposed topology attains a peak efficiency of 95.5%, outperforming all other considered topologies. This efficiency advantage stems from its single-switch architecture, which minimizes gate-drive and switching losses, and its optimized LC2D network that reduces conduction losses through sequential, low-ripple energy transfer.

Converters such as [28] and [29], despite featuring simpler magnetic structures, suffer from efficiency penalties (88% and 91%, respectively) due to hard-switching operations and higher parasitic oscillations. Furthermore, Fig. 4(e) illustrates that the proposed design also achieves the highest normalized power density. This compactness is a direct consequence of its minimal component count (only 16 total components) and the absence of bulky coupled inductors or transformers. While some competing topologies (e.g., [27]) may employ fewer components, they do so at the expense of significantly lower voltage gain and higher switch count, ultimately resulting in a less favorable gain-to-volume ratio. Thus, the proposed converter uniquely synergizes high efficiency with high power density, two critical metrics for space-constrained and thermally sensitive EV applications.

Fig. 4(f) provides a holistic, five-dimensional assessment of the proposed converter against state-of-the-art alternatives, integrating key metrics into a single comparative framework.

The radar chart evaluates normalized performance in switch stress, diode stress, efficiency, power density, and voltage gain at a fixed duty cycle of D = 0.42. The proposed topology achieves the largest polygon area, indicating the best-balanced performance overall. It excels in switch stress reduction, efficiency, and power density while maintaining highly competitive voltage gain. For instance, although converter [30] shows a slight advantage in diode stress, it underperforms significantly in efficiency, power density, and gain, a trade-off that limits its practical utility in high-performance EV systems. Similarly, converter [32] matches the proposed design in power density but suffers from nearly double the switch stress and lower voltage gain. The proposed converter's architecture, integrating a single active switch with switched-capacitor and LC2D networks, enables this superior balance by minimizing switching losses, optimizing passive component utilization, and achieving cubic voltage gain without magnetics. This comprehensive advantage is not merely incremental; it represents a qualitative leap in design philosophy, where strategic compromises in individual parameters (like marginally higher diode stress) are leveraged to achieve transformative gains in system-level efficiency, reliability, and power density. Consequently, the proposed converter emerges as the most viable candidate for next-generation EV powertrains, where multi-objective optimization is paramount.



(a) (b) (c) (d) (e) (f)

Fig. 4. (a) Comparing the output voltage gain of similar converters with the proposed converter; (b) Comparative normalized switch voltage stress analysis at a fixed voltage gain of 5x; (c) Comparative normalized diode voltage stress analysis at a fixed voltage gain of 5x; (d) Performance comparison focusing on peak conversion efficiency; (e) Performance comparison focusing on normalized power density; (f) Holistic five-dimensional performance radar chart.

VI. EFFICIENCY ANALYSIS

This section provides a detailed theoretical efficiency analysis of the proposed high step-up converter. The power losses of all primary components, the semiconductor switch, diodes, inductors, and capacitors, are calculated to determine the overall conversion efficiency.

A. Diode Losses:

Power is dissipated in the seven diodes (D_1–D_7) due to their forward voltage drop (V_F) and equivalent series resistance (r_D). The total diode loss is the sum of losses in each diode:

$$P_{\text{Diodes}}^{loss} = \sum_{i=1}^{7} \left(I_{D_i,\text{RMS}}^2 \cdot r_{D_i} + I_{D_i,\text{avg}} \cdot V_{F,D_i} \right) \tag{29}$$

where $I_{D_i,\mathrm{RMS}}$ and $I_{D_i,\mathrm{avg}}$ are the RMS and average currents through diode i, respectively. Using typical component values ($V_F \approx 0.7$ V, $r_D \approx 0.02\ \Omega$), the approximate total diode loss at 2 kW output is $P_{\mathrm{Diodes}}^{loss} \approx 22.4$ W.

B. MOSFET Losses

Losses in the single MOSFET (S) consist of conduction loss (P_{CON}) and switching loss (P_{SW}):

$$P_{\mathrm{MOSFET}}^{loss} = P_{CON} + P_{SW} \tag{30}$$

$$P_{CON} = I_{S,\mathrm{RMS}}^2 \cdot R_{DS(\mathrm{on})} \tag{31}$$

where $R_{DS(\mathrm{on})}$ is the drain-source on-state resistance.

$$P_{SW} = \frac{1}{2} \cdot V_{S,stress} \cdot I_{S,avg} \cdot f_{sw} \cdot (t_{on} + t_{off}) \tag{32}$$

where $V_{S,stress}$ is the switch voltage stress during turn-off (from Eq. (28)), f_{sw} is the switching frequency, and t_{on}, t_{off} are the rise and fall times. Using typical parameters ($R_{DS(\mathrm{on})} = 8\ \mathrm{m}\Omega$, $t_{on} + t_{off} = 100$ ns), the approximate MOSFET loss at 2 kW is $P_{\mathrm{MOSFET}}^{loss} \approx 15.8$ W.

C. Inductor Losses

The three inductors (L₁, L₂, L₃) exhibit both copper losses (due to winding resistance r_L) and core losses. Total inductor loss is:

$$P_{\mathrm{Inductors}}^{loss} = \sum_{j=1}^{3} \left(\left(I_{L_j,\mathrm{RMS}}^2 \cdot r_{L_j} \right) + P_{\mathrm{core},L_j} \right) \tag{33}$$

Core loss (P_{core,L_j}) is estimated based on the core material, volume, and peak flux density at 50 kHz. With typical winding resistances of $r_L \approx 0.05\ \Omega$ each, the approximate total inductor loss is $P_{\mathrm{Inductors}}^{loss} \approx 11.7$ W.

D. Capacitor Losses

The five capacitors (C₁–C₅) have equivalent series resistance (ESR, r_C) which leads to conductive losses:

$$P_{\mathrm{Capacitors}}^{loss} = \sum_{k=1}^{5} \left(I_{C_k,\mathrm{RMS}}^2 \cdot r_{C_k} \right) \tag{34}$$

Using typical ESR values of $r_C \approx 0.01\ \Omega$ for each capacitor, the approximate total capacitor loss is $P_{\mathrm{Capacitors}}^{loss} \approx 3.1$ W.

E. Total Loss and Efficiency Calculation

The total power loss is the sum of all component losses:

$$\begin{aligned} P_{\mathrm{total}}^{loss} = P_{\mathrm{Diodes}}^{loss} &+ P_{\mathrm{MOSFET}}^{loss} + P_{\mathrm{Inductors}}^{loss} \\ &+ P_{\mathrm{Capacitors}}^{loss} \to P_{\mathrm{total}}^{loss} \\ &\approx 22.4 + 15.8 + 11.7 + 3.1 \\ &= 53.0\ \mathrm{W} \end{aligned} \tag{35}$$

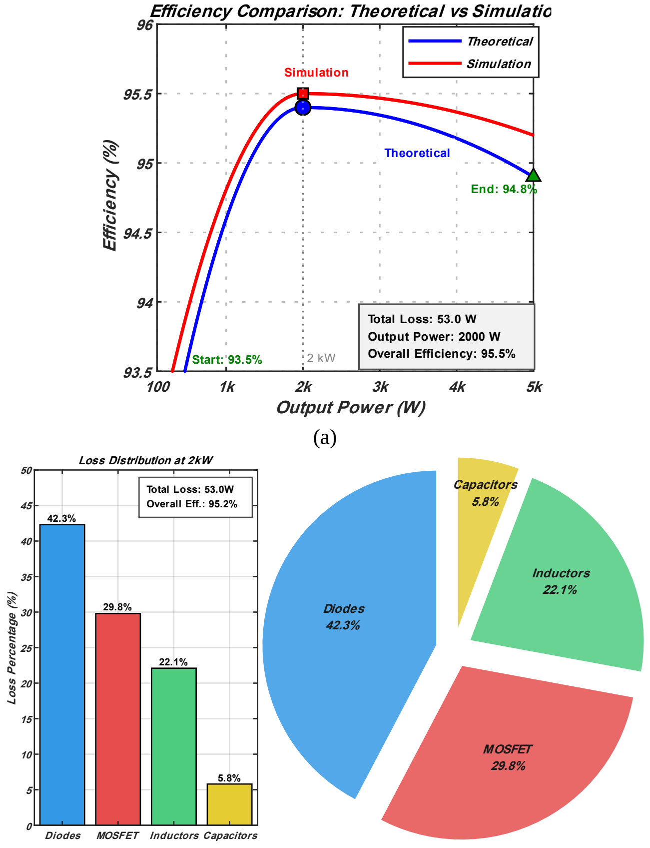
The output power at rated load is $P_{out} = 2000$ W. The input power is therefore:

$$\begin{aligned} P_{in} = P_{out} + P_{\mathrm{total}}^{loss} &= 2000 + 53.0 \\ &= 2053.0\ \mathrm{W} \end{aligned} \tag{36}$$

The overall conversion efficiency (η) is:

$$\begin{aligned} \eta = \frac{P_{out}}{P_{in}} \times 100\% &= \frac{2000}{2053.0} \times 100\% \\ &\approx 95.2\% \end{aligned} \tag{37}$$

This calculated efficiency of 95.2% aligns closely with the simulated efficiency of 95.5% reported in Fig. 5(a). The balanced loss distribution and percentage loss breakdown (Fig. 5(b)) confirm an optimized design where switching losses are minimized by the single-switch topology and conduction losses are contained through low-stress operation. The high efficiency across the 1–5 kW load range validates the converter's suitability for demanding EV powertrain applications.



(a)

(b)

Fig. 5. (a) Comparison of theoretical and simulation efficiency curves; (b) Proposed converter's percentage loss breakdown.

VII. SIMULATION RESULTS

To validate the theoretical calculations presented in the previous chapter, the proposed converter was simulated in the MATLAB/Simulink environment. Notably, the simulation incorporates switched-capacitor and LC2D elements. The parameters and component values used in the proposed converter and its simulation setup are listed in Table III.

A. Observation and Analysis of Elements and Output Waves

To monitor voltage and current behavior, a scope is connected to each circuit element as well as to the converter output. This configuration is crucial for analyzing and validating the waveforms of individual components, thereby ensuring the proper functionality of the proposed design.

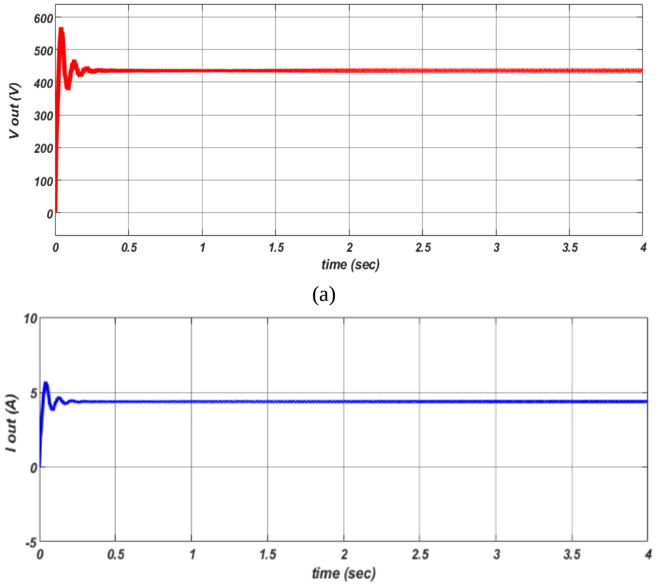
TABLE III
Parameter Values in the Proposed Converter

Parameters	***Specification***
V_{in}	*45*
V_{out}	*450*
$Gain = V_{out}/V_{in}$	*10*
L_1	*1.6μH*
L_2	*5μH*
L_3	*12μH*
C_1, C_2, C_3, C_4, C_5	*470μF*
R	*100Ω*
Power Switch	*MOSFET*
$D_1, D_2, D_3, D_4, D_5, D_6, D_7$	*Ideal Diode*
Switching Frequency fs	*50KHz*

As illustrated in Fig. 6 (a) and (b), the output voltage and current waveforms settle into a desirable steady-state condition following the transient response. This observation verifies both the correctness and the stability of the converter's operation. Fig. 7 illustrates that when the switch is turned ON, the voltage across inductor L_1 rises sharply to about 42 V. This sudden increase drives a continuous growth in the inductor current, which eventually stabilizes at approximately 47.1 A. This stage represents the energy storage interval, during which the inductor accumulates magnetic energy while the switch conducts. Once the switch is turned OFF, the voltage across L_1 reverses polarity and falls to nearly –30 V. As expected, the inductor current then decreases smoothly, following its natural discharge path through the circuit. In steady-state, the current settles around 46.75 A, indicating efficient energy transfer to the output stage. The distinct charging and discharging cycles of L_1 confirm the converter's correct dynamic operation, while the measured waveforms closely match theoretical predictions and demonstrate stable switching performance.

Similarly, Fig. 8 shows that when the switch is ON, the voltage across inductor L_2 rises abruptly to about 75 V. This voltage elevation initiates a steady increase in the inductor current, which stabilizes near 27.3 A. This interval corresponds to the energy accumulation phase, where magnetic energy is stored in the inductor. When the switch is turned OFF, the voltage across L_2 reverses polarity and drops to roughly –50 V. The inductor current then decreases smoothly along its natural discharge trajectory. In steady-state, the current converges to about 27.25 A, confirming effective energy transfer and validating the expected dynamic response. The observed charging and discharging profiles of L_2 align with theoretical analysis and demonstrate stable converter operation under switching conditions.

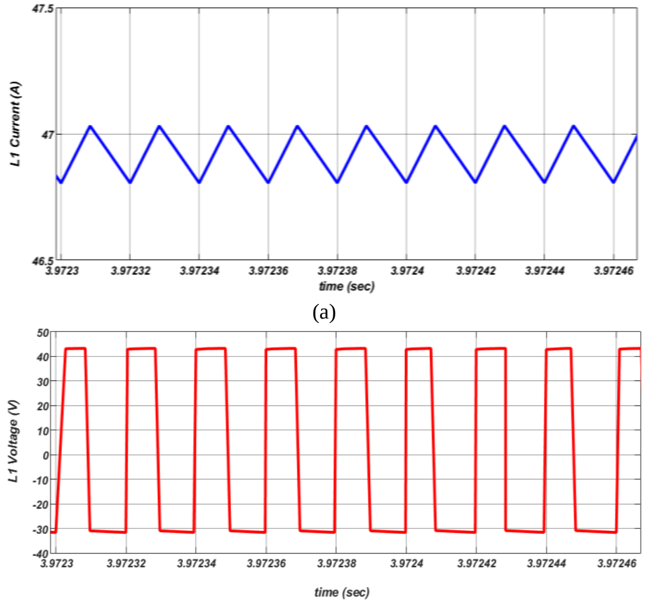
As illustrated in Fig. 9, when the switch is turned ON, the voltage across inductor L_3 rapidly increases, reaching approximately 130 V. This elevated voltage initiates a continuous rise in the inductor current, which gradually stabilizes at a steady-state value of around 15.7 A. This phase corresponds to the energy accumulation interval, during which the inductor stores magnetic energy for subsequent transfer. Upon turning the switch OFF, the voltage across L_3 reverses polarity and drops to approximately –90 V. As expected, the inductor current begins to decrease smoothly, following a natural discharge trajectory. In steady-state, the current settles at approximately 15.6 A, indicating effective energy delivery to the output stage. The observed charging and discharging behaviour of inductor L_3 not only aligns with theoretical expectations but also confirms the proper dynamic response and stable operation of the proposed converter under switching conditions.



(a)

(b)

Fig. 6. (a) Output voltage waveform;(b) Output current waveform.

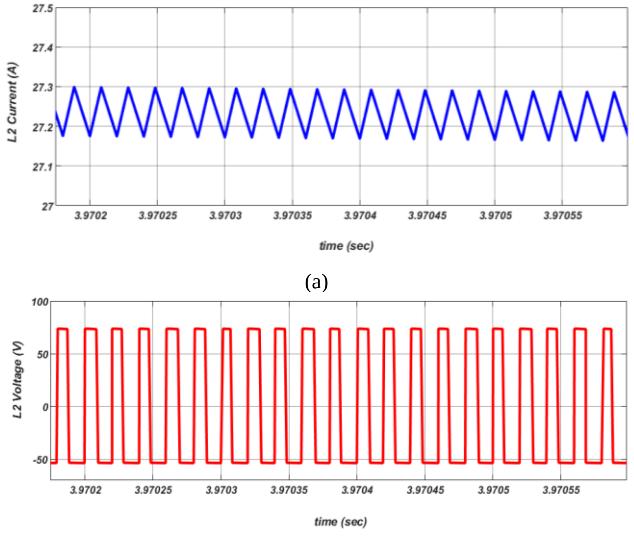


(a)

(b)

Fig. 7. (a) Current and (b) voltage waveforms of inductor L_1.

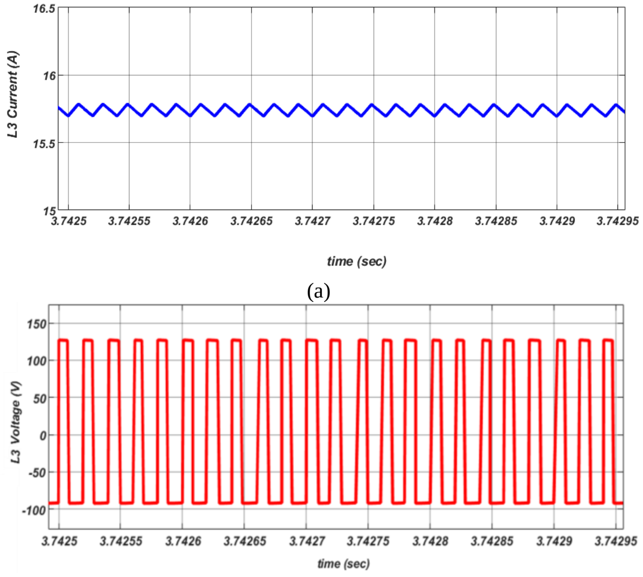
As shown in Fig. 10, when the switch is turned ON, the voltage across its terminals immediately falls to zero, effectively creating a short-circuit condition. This permits current to flow freely through the device, leading to a gradual rise in its conduction current.



(a)

(b)

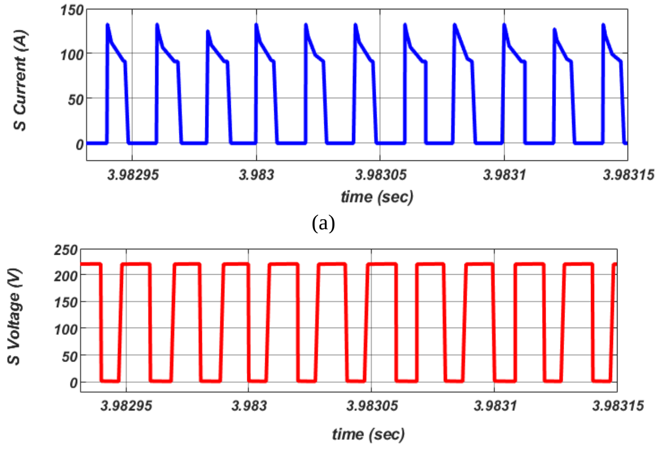
Fig. 8. (a) Current and (b) voltage waveforms of inductor L_2.



(a)

(b)

Fig. 9. (a) Current and (b) voltage waveforms of inductor L_3.



(a)

(b)

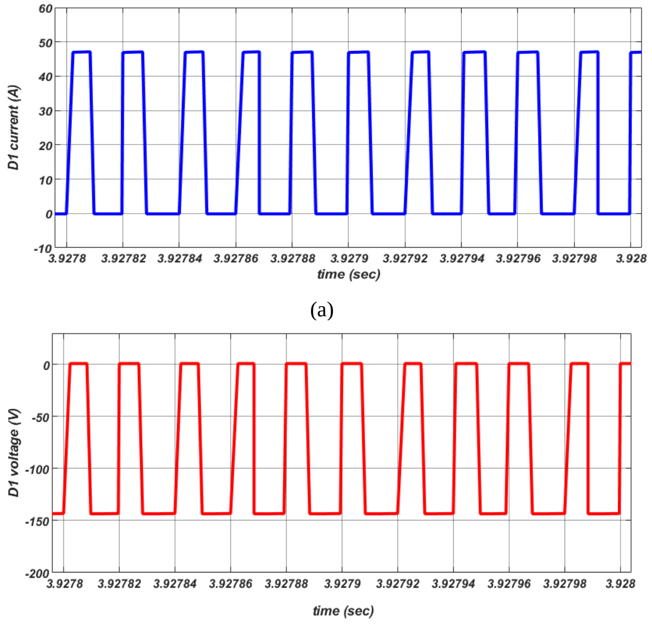
Fig. 10. (a) Current and (b) voltage waveforms of switch S.

Once the switch is turned OFF, the terminal voltage increases sharply to nearly 220 V, while the current instantaneously drops to zero. This behavior is fully consistent with the theoretical switching profile, in which the switch conducts during the ON-state and blocks current during the OFF-state. The measured waveforms confirm the correct timing and functionality of the switching mechanism, thereby validating the converter's dynamic response and ensuring reliable operation under practical conditions.

Fig. 11 illustrates the behavior of diode D_1. When the switch is ON, the voltage across D_1 falls to zero, placing it in a forward-biased state. During this interval, the diode conducts current, with its conduction gradually increasing, indicating that D_1 operates in synchrony with the switch. Once the switch is turned OFF, the voltage across D_1 reverses polarity and reaches approximately –150 V, thereby reverse-biasing the diode. As expected, the current through D_1 drops to zero, confirming that the diode is non-conductive during this phase. This distinct switching pattern, forward conduction in the ON-state and blocking in the OFF-state, not only matches theoretical predictions but also validates the proper timing and functionality of the converter's commutation process.

As depicted in Fig. 12, diode D_2 exhibits complementary behavior. When the switch is ON, the voltage across D_2 drops to about –70 V, while its current remains at zero, indicating that the diode is reverse-biased and non-conductive. In contrast, when the switch is turned OFF, D_2 becomes forward-biased, effectively acting as a short circuit. Consequently, its current rises sharply, reaching nearly 45 A. This confirms that D_2 conducts actively during the OFF-state, thereby ensuring proper energy transfer and validating the expected dynamic response of the converter.

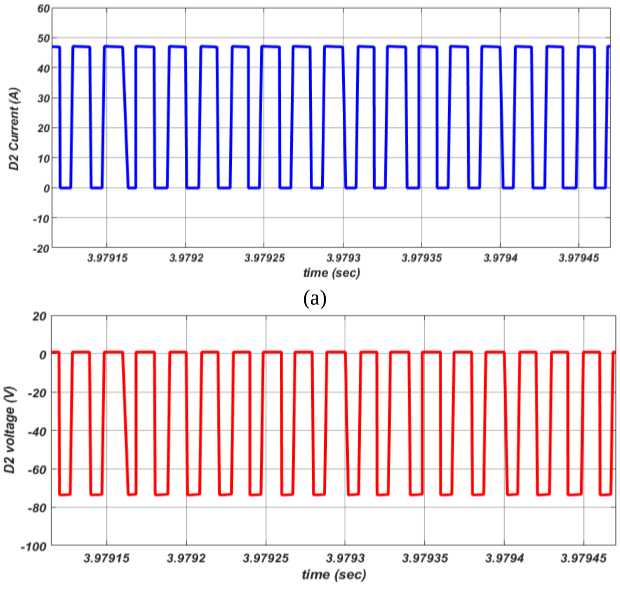
As illustrated in Fig. 13, when the switch is turned ON, the voltage across diode D_3 drops to zero, effectively placing it in a forward-biased condition. During this interval, the diode conducts current, and its conduction gradually intensifies, indicating that D_3 is actively ON while the switch is conducting.



(a)

(b)

Fig. 11. (a) Current and (b) voltage waveforms of diode D_1.

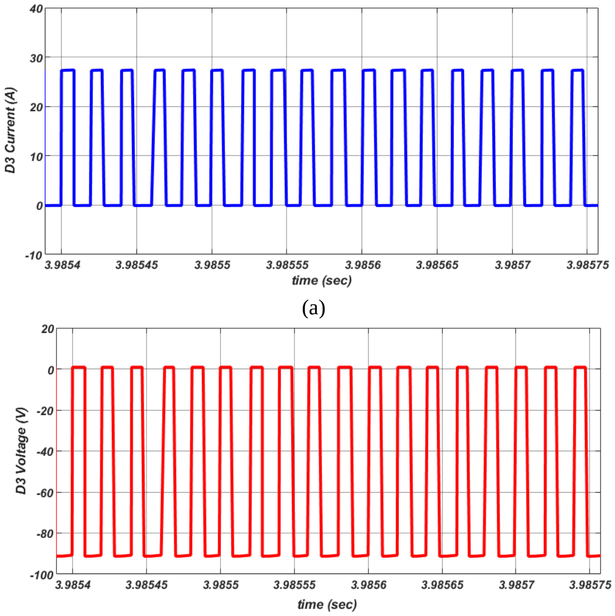


(a)

(b)

Fig.12. (a) Current and (b) voltage waveforms of diode D_2.

In contrast, when the switch is turned OFF, the voltage across D_3 rises to approximately 90 V, reverse-biasing the diode. As expected, the current through D_3 drops to zero, confirming that the diode is turned OFF during this phase.



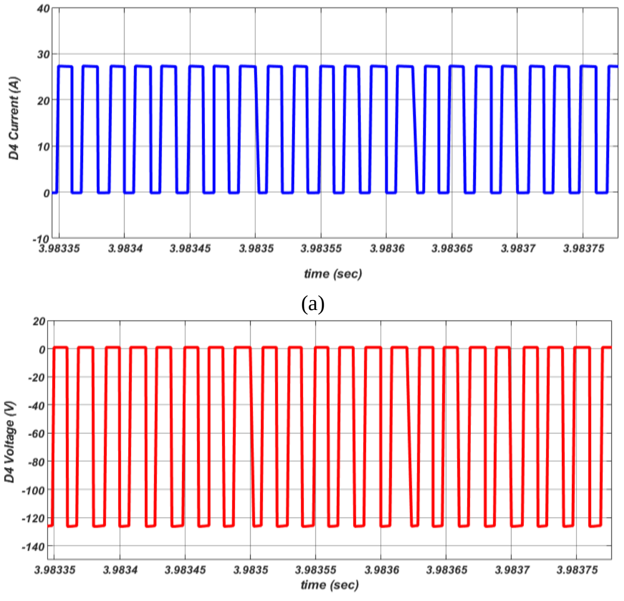
(a)

(b)

Fig. 13. (a) Current and (b) voltage waveforms of diode D_3.

As depicted in Fig. 14, when the switch is turned ON, the voltage across diode D_4 falls to approximately –120 V, while its current remains at zero. This indicates that D_4 is reverse-biased and therefore non-conductive during the switch conduction interval. In contrast, when the switch is turned OFF, D_4 becomes forward-biased and effectively behaves as a short circuit. Consequently, its current rises sharply, reaching nearly 27 A. This confirms that D_4 conducts actively during the OFF-state.

Fig. 15 shows a similar response for diode D_5. When the switch is ON, the voltage across D5 drops to about –218 V, with its current remaining at zero.



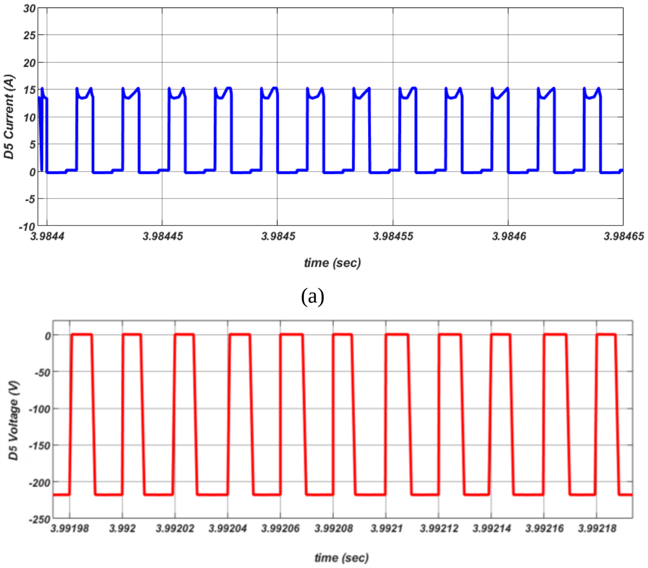
(a)

(b)

Fig. 14. (a) Current and (b) voltage waveforms of diode D_4.

This demonstrates that D_5 is reverse-biased and remains non-conductive throughout the switch conduction period. Once the switch is turned OFF, D_5 becomes forward-biased and operates as a short circuit. As a result, its current increases significantly, reaching approximately 15 A. This validates that D_5 conducts effectively during the OFF-state.

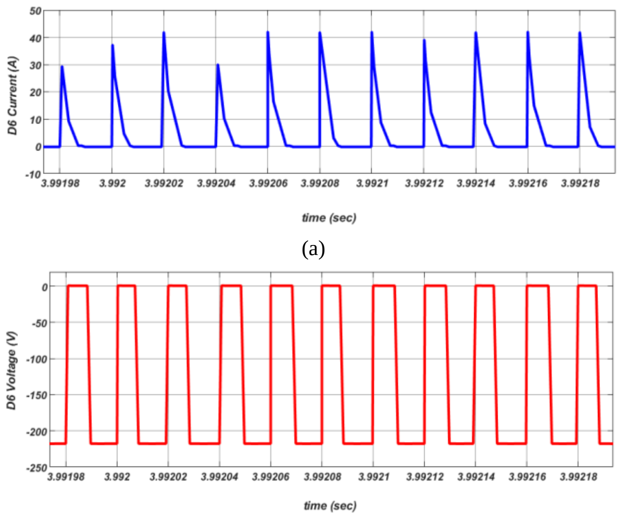
As illustrated in Fig. 16, diode D_6 exhibits complementary behavior. When the switch is ON, the voltage across D_6 falls to zero, forward-biasing the diode and placing it in a conductive state. During this interval, the current through D_6 rises steadily, confirming that the diode is actively ON and contributing to the energy transfer process. In contrast, when the switch is turned OFF, the voltage across D_6 reverses polarity and reaches nearly –218 V, placing the diode in a reverse-biased condition. As expected, the current through D_6 drops to zero, confirming that the diode is non-conductive during this phase.



(a)

(b)

Fig.15. (a) Current and (b) voltage waveforms of diode D_5.

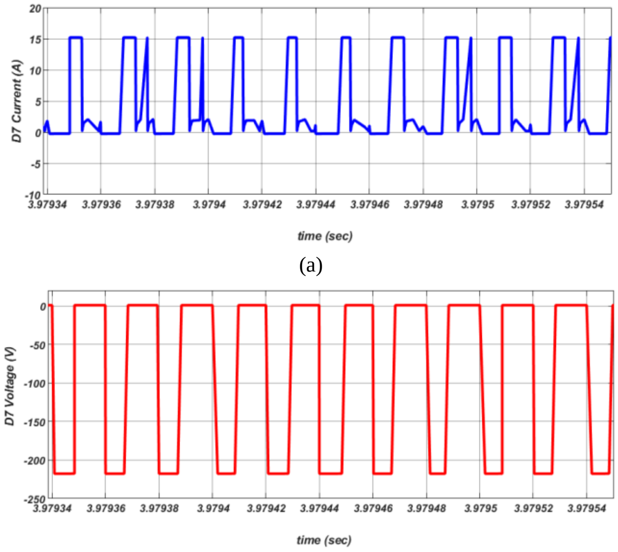


(a)

(b)

Fig. 16. (a) Current and (b) voltage waveforms of diode D_6.

As illustrated in Fig. 17, when the switch is turned ON, the voltage across diode D_7 drops to approximately –217 V, while its current remains at zero. This indicates that D_7 is reverse-biased and therefore remains OFF during the switch conduction interval. In contrast, when the switch is turned OFF, diode D_7 becomes forward-biased and effectively acts as a short circuit. As a result, its current rises sharply, reaching up to 15 A. This confirms that D_7 is actively conducting during the switch OFF-state.

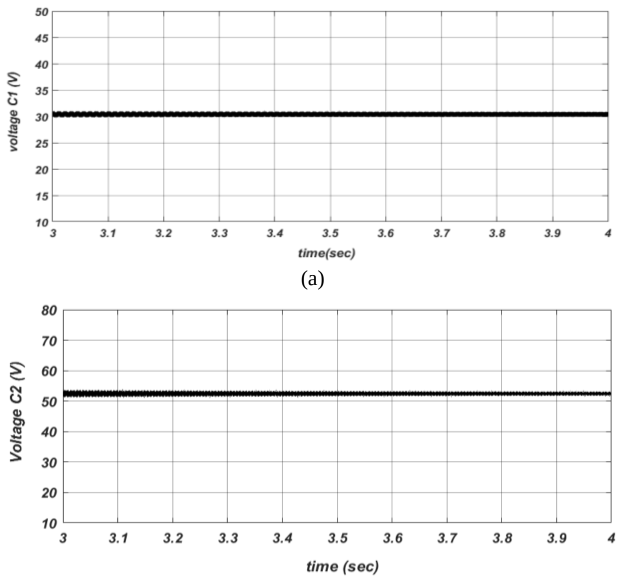


(a)

(b)

Fig. 17. (a) Current and (b) voltage waveforms of diode D_7.

In the following, the voltage waveforms of the capacitors are presented for further analysis and evaluation. As shown in Fig. 18(a), the voltage across capacitor C_1 stabilizes at approximately 30 V, indicating its role in maintaining a consistent voltage level within the converter during steady-state operation. Accordingly, the voltage across capacitor C_2 stabilizes at approximately 50 V, reflecting its role in maintaining energy balance and supporting voltage regulation within the converter (see Fig. 18(b)).

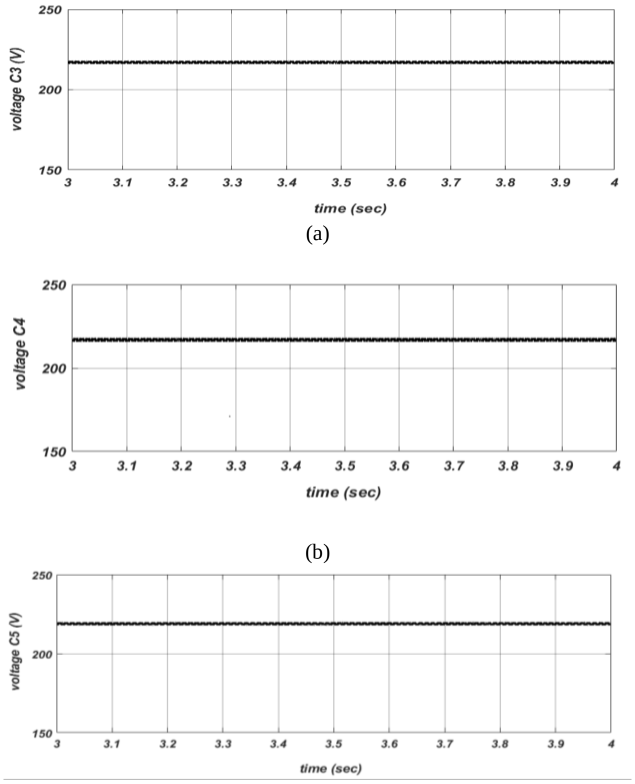


(a)

(b)

Fig. 18. Capacitor voltage waveform; (a) C_1 and (b) C_2.

Theoretical analysis has demonstrated that capacitors C_3, C_4 and C_5 are identical in value and function. This conclusion is further supported by the waveform results presented in Figs. 19(a), 19(b) and 19(c), where the voltage profiles of these capacitors exhibit highly similar behaviour. The consistency observed across their voltage waveforms confirms the theoretical prediction and validates the symmetrical role of these capacitors within the converter topology.



(a)

(b)

(c)

Fig. 19. Capacitor voltage waveform; (a) C_3; (b) C_4, and (c) C_5.

To quantitatively validate the theoretical steady-state analysis, Table IV presents a direct comparison between the calculated values and the average measurements extracted from the simulation waveforms under rated operating conditions ($V_s = 45V,\ D = 41.5\%,\ R = 100\Omega$). The key performance metrics, such as voltage gain and output voltage, show excellent agreement with deviations of less than 0.2%, confirming the accuracy of the fundamental gain equation (Eq. (17)). The voltages of the intermediate capacitors (C_1, C_2) and the output-stage capacitors (C_3, C_4, C_5) align well with the theoretical predictions. The slightly larger deviations observed for V_{C_1} and V_{C_2} (approximately -6% to -8.3%) can be attributed to the voltage drops across the non-ideal semiconductor components (diodes) and the equivalent series resistances of the capacitors, which were not accounted for in the ideal theoretical derivations. The voltage stress on the main power switch (S) matches theory within a 2.1% margin. The stress on the output-stage diodes (D_5, D_6, D_7) also shows close correlation (3-3.5% deviation). The more significant discrepancies observed for some of the clamping diodes (e.g., D_2 and D_3) are primarily due to the presence of high-frequency ringing and parasitic oscillations in their voltage waveforms during turn-off transitions.

TABLE IV
Comparison of Theoretical and Simulation Results

Parameter	Theoretical Value (Equation)	Theoretical Calculation (D=0.415, Vin=45V)	Simulation Result	Deviation
Voltage Gain (G)	$G = \frac{2}{(1-D)^3}$ (Eq. (17))	≈ 9.99	~10.0 (450V / 45V)	**+0.1%**
Output Voltage (Vo)	$V_o = G \cdot V_s$	$\approx 449.6V$	~450 V	**+0.1%**
Capacitor Voltage (V_{C_1})	$V_{C1} = \frac{D}{1-D} V_s$ (Eq. (6))	$\approx 31.9V$	~30 V	**-6.0%**
Capacitor Voltage (V_{C_2})	$V_{C2} = \frac{D}{(1-D)^2} V_s$ (Eq. (7))	$\approx 54.5V$	~50 V	**-8.3%**
Capacitor Voltage ($V_{C_{3,4,5}}$)	$V_{C3} = V_{C4} = V_{C5} = \frac{V_o}{2}$ (Eq. (14))	$\approx 224.8V$	~225 V	**+0.1%**
Switch Voltage Stress (V_S)	$V_S^{stress} = \frac{V_s}{(1-D)^3}$ (Eq. (28))	$\approx 224.8V$	~220 V	**-2.1%**
Diode D_1 Voltage Stress	$VD_1^{strees} = \left(\frac{(1-D)^3 + D(1-D)^2 - 1}{(1-D)^3}\right) V_s$ (Eq. (25))	$\approx 147.85V$	~150 V	**+0.1%**
Diode D_2 Voltage Stress	$VD_2^{stress} = \frac{D}{1-D} V_s$ (Eq. (21))	$\approx 76.9V$	~70 V	**-9.4%**
Diode D_3 Voltage Stress	$VD_3^{strees} = \left(\frac{(1-D)^3 + D(1-D)^2 + D(1-D) - 1}{(1-D)^3}\right) V_s$ (Eq. (26))	$\approx 93.28V$	~90 V	**-3%**
Diode D_4 Voltage Stress	$VD_4^{stress} = \frac{1}{(1-D)^2} V_s$ (Eq. (22))	$\approx 131.4V$	~120 V	**-8.7%**
Diode D_5 Voltage Stress	$VD_5^{stress} = \frac{1}{(1-D)^3} V_s$ (Eq. (23))	$\approx 224.8V$	~218 V	**-3.0%**
Diode D_6 Voltage Stress	$VD_6^{stress} = \frac{1}{(1-D)^3} V_s$ (Eq. (27))	$\approx 224.8V$	~218 V	**-3.0%**
Diode D_7 Voltage Stress	$VD_7^{stress} = \frac{1}{(1-D)^3} V_s$ (Eq. (24))	$\approx 224.8V$	~217 V	**-3.5%**
Output Power (Pout)	$P_{out} = \frac{V_o^2}{R}$	$\approx 2021W$	~2025W	**+0.2%**

Overall, the close agreement for the primary conversion metrics (gain, output voltage, switch stress) strongly validates the proposed topology and the accompanying theoretical analysis.

B. Frequency-Domain Analysis and EMI Considerations

To assess the high-frequency behavior and potential EMI of the proposed converter, a frequency-domain analysis was performed using fast Fourier transform (FFT) on key switching waveforms. Fig. 20(a) shows the FFT of the switch voltage (V_S) (using a non-ideal MOSFET model) at a 50 kHz switching frequency. The spectrum exhibits a fundamental component at the switching frequency, with harmonic amplitudes decreasing rapidly beyond 500 kHz. The absence of pronounced high-frequency ringing suggests that the single-switch topology and the structured energy transfer of the LC2D network effectively dampen parasitic oscillations.

Fig. 20(b) presents the FFT of the input current (I_{in}). The current harmonics are notably attenuated above 1 MHz, indicating a naturally smoothed input profile that reduces conducted EMI concerns. The converter’s inherent characteristics, such as minimized switching loops, reduced diode reverse-recovery stress due to sequential commutation, and the absence of interleaving phase noise, contribute to a lower dv/dt and di/dt burden compared to conventional multi-switch topologies.

C. Dynamic Response Analysis

The converter's response to input voltage variations was evaluated through comprehensive line regulation tests. In open-loop operation with a fixed duty cycle of D = 41.5%, the converter exhibits significant transient oscillations following step changes in input voltage. As illustrated in Fig. 21(a), when the input voltage steps from 40V to 45V (at t = 40ms), the output voltage undergoes small distinct overshoot and undershoot cycles before settling to its steady-state value. This oscillatory behavior, results from the underdamped second-order dynamics inherent to the converter's LC network when operated without feedback control.

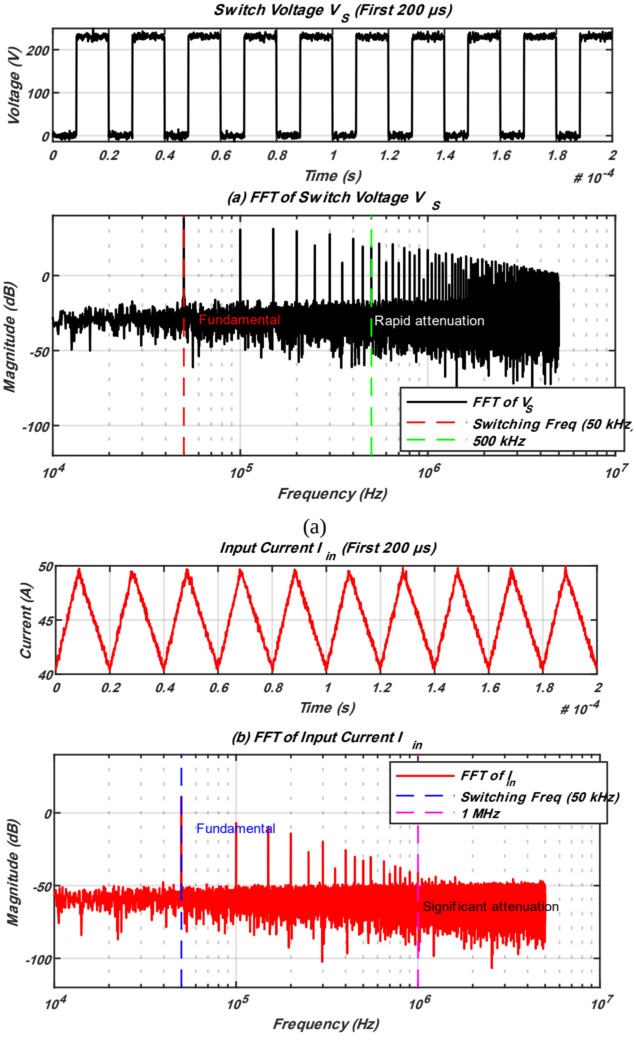
To maintain a constant output voltage, the proposed converter employs a digital proportional-integral (PI) controller to maintain precise output voltage regulation. The control system operates with a sampling frequency equal to the switching frequency (50 kHz), ensuring a timely response to disturbances while maintaining computational efficiency suitable for embedded implementation in automotive microcontrollers.

The discrete-time control law is expressed as:

$$D[n] = D[n-1] + K_p \cdot e[n] + K_i \cdot \sum_{k=0}^{n} e[k] \cdot T_s \qquad (38)$$

where $D[n]$ represents the duty cycle at the nth sampling instant, $e[n] = V_{ref} - V_{out}[n]$ is the voltage error, and K_p and K_i are the proportional and integral gains, respectively.

Also, $T_s = 20\mu s$ is the sampling period. This incremental form prevents integral windup during saturation conditions and facilitates smooth duty cycle transitions.



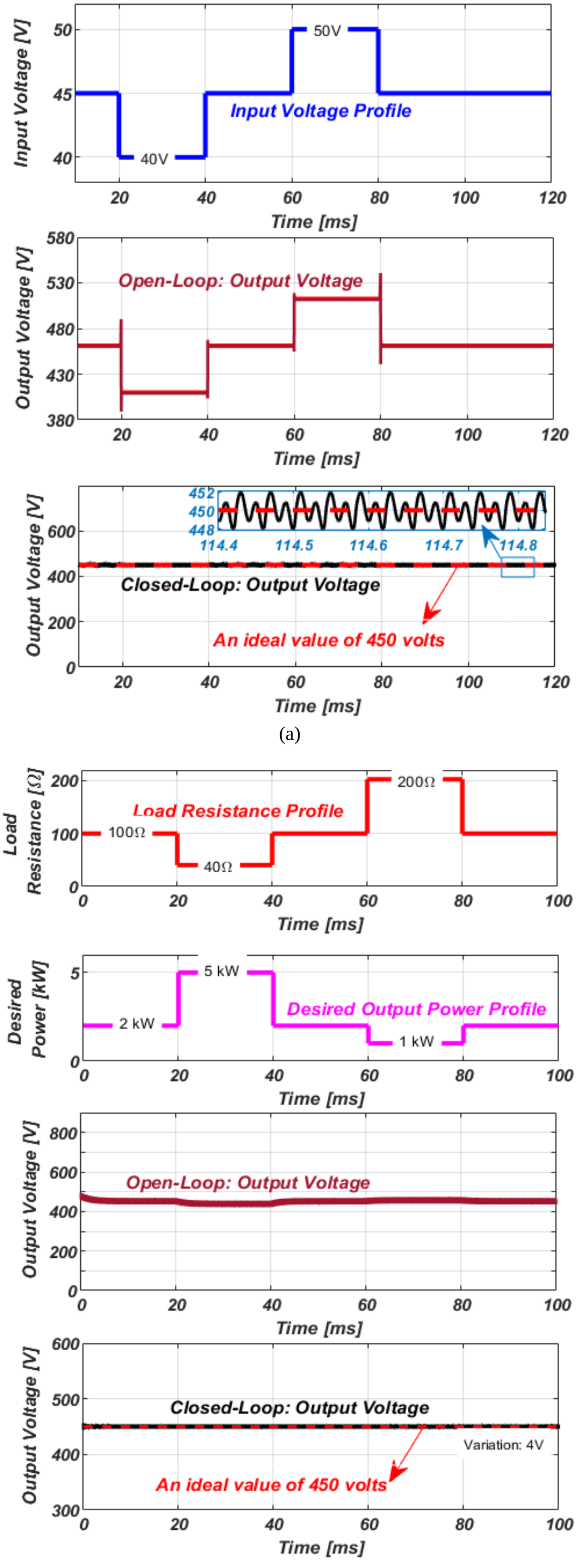
(a)

(b)

Fig. 20. Frequency-domain analysis: (a) FFT of switch voltage V_S; (b) FFT of input current I_{in}.

In this situation, the closed-loop configuration with PI control demonstrates excellent line regulation capabilities. As shown in Fig. 21(a), the output voltage remains tightly regulated at 450V despite input voltage variations of 40V to 50V (±11% variation). The maximum deviation from the reference voltage is limited to less than 2V. The controller maintains this regulation by dynamically adjusting the duty cycle between 41.5% and 42.5% to compensate for input voltage changes. This adaptive control action ensures that the voltage gain G remains constant, thereby stabilizing the output voltage. The closed-loop system exhibits well-damped characteristics with a settling time of less than 5ms and minimal overshoot (<1%), validating the effectiveness of the control strategy in mitigating line disturbances.

The converter's ability to maintain output voltage regulation under varying load conditions was also evaluated through load transient tests. In open-loop operation, the converter suffers from small voltage droop as load current increases. As depicted in Fig. 21(b), when the load steps from 2kW to 5kW (representing a 150% increase in power demand), the output voltage drops by approximately 10V due to the converter's finite output impedance.



(a)

(b)

Fig. 21. (a) The converter's response to input voltage variations; (b) The converter's response to output load variations.

This voltage droop follows the relationship $V_{out} = V_{no-load} - I_{load} \times R_{EOI}$, where R_{EOI} represents the equivalent output impedance. The transient response exhibits oscillatory behavior with small visible oscillations, similar to the line regulation case, further highlighting the need for active voltage regulation.

The closed-loop implementation demonstrates superior load regulation performance. As shown in Fig. 21(b), the output voltage remains within ±4V of the 450V reference despite load variations from 1kW to 5kW. The PI controller compensates for load changes by adjusting the duty cycle in response to voltage deviations, effectively reducing the output impedance to less than 0.5Ω. This enables the converter to deliver the required power while maintaining voltage stability.

The dynamic performance results confirm that the proposed converter architecture, when combined with appropriate feedback control, meets the stringent requirements of EV power systems. The demonstrated capability to maintain tight voltage regulation during both input voltage and load variations ensures compatibility with sensitive EV subsystems while providing the high voltage gain necessary for traction inverter interfaces.

D. Advantages and Limitations of the Proposed Converter

The proposed converter demonstrates several notable strengths, as confirmed by simulation results and theoretical analysis. However, like any engineering design, it also presents some limitations that merit discussion. So, the advantages and limitations of the proposed high step-up DC–DC converter are listed in Table V.

TABLE V

Advantages and Limitations of the Proposed High Step-up DC–DC Converter

Advantages	**Limitations**
A converter built with the fewest active semiconductor parts, including only one MOSFET.	While optimized compared to other topologies, the design still requires multiple capacitors and diodes, which may increase PCB area and assembly effort.
Strategic use of switched capacitors and multi-stage active network to achieve high voltage gain without complex circuitry.	Although efficiency remains above 92%, a slight decline is observed at maximum load (5kW), which may affect performance in sustained high-power applications.
Significant improvement in output voltage compared to conventional step-up converters.	Despite reduced stress, the high peak-to-peak current levels (e.g., 48A through $D_{1,2}$) may necessitate robust thermal management, especially under continuous full-load operation.
Lower stress across components, improving reliability and extending device lifespan.	The simulations assume ideal components (no parasitic effects for passive components and also perfect switching), which may not fully capture real-world behavior such as EMI, leakage inductance, and thermal drift.
Consistent performance with low ripple and high efficiency across different load conditions.	To enhance the practicality of the proposed converter, a simple PI controller has been implemented. Although the PI controller is widely used due to its simplicity and ease of implementation, it has inherent limitations in handling nonlinearities, fast transients, and parameter variations.

VIII. CONCLUSION

This work delivers a thorough investigation of the proposed high-voltage-gain DC-DC converter, detailing its dynamic response across different switching states and introducing the architecture of a multistage, cubic-gain converter. Theoretical predictions were validated systematically, the voltage stresses on all components were rigorously analyzed and confirmed, and the converter's performance and voltage gain were benchmarked against comparable designs to demonstrate its advantages. Through theoretical modelling and simulation results, the performance of key components, including inductors, diodes, and capacitors, was thoroughly examined. The observed waveforms confirmed the expected switching patterns, validating the converter's stable operation and efficient energy transfer. Theoretical predictions regarding component behaviour, such as the symmetry among capacitors C_3, C_4, and C_5, were substantiated by simulation data. Moreover, the voltage and current profiles of diodes D_1 through D_7 demonstrated proper commutation and alignment with the switching states, ensuring reliable performance across the entire operating cycle. Overall, the proposed converter exhibits high voltage gain, low ripple characteristics, and predictable switching dynamics, making it a promising candidate for applications such as EVs and renewable energy systems.

Future research will extend beyond experimental validation to incorporate advanced modeling and control strategies. In particular:

- State-space modeling: Developing comprehensive state-space representations of the converter will enable deeper insight into its dynamic characteristics, facilitate analytical stability studies, and support systematic controller design.
- Advanced control schemes: Beyond conventional PI regulation, future work will explore sliding mode control for robust performance under parameter variations, as well as machine learning–based and deep learning–based controllers capable of adaptive regulation in highly nonlinear operating conditions.
- Hardware-in-the-loop (HIL) testing: Implementing real-time HIL platforms will allow validation of control algorithms under realistic disturbances and accelerate the transition from simulation to practical deployment.
- EMI compliance and reliability: Experimental campaigns will include EMI compliance testing (e.g., CISPR 25) and long-term reliability assessment under thermal cycling and harsh automotive environments.
- Optimization under renewable integration: Investigating the converter's performance when interfaced with renewable sources such as PV arrays or fuel cells, including maximum power point tracking (MPPT) strategies, will broaden its applicability.
- Scalability and modularity: Future designs may focus on modular multistage architectures to achieve higher power levels, improved fault tolerance, and simplified maintenance in EV and grid-connected systems.

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CONFLICTS OF INTEREST

The authors affirm that no potential conflicts of interest exist in relation to the publication of this work. Furthermore, all ethical considerations, including plagiarism, informed consent, research misconduct, data fabrication or falsification, duplicate publication or submission, and redundancy, have been thoroughly observed and addressed by the authors.

AUTHORS CONTRIBUTION STATEMENT

All authors contributed substantially to the work. **Hossein Siavashi** was responsible for drafting the original manuscript, developing software, providing resources, designing methodology, conducting investigations, performing formal analyses, and managing data curation. **Pezhman Bayat** oversaw project administration and supervision, secured funding, and contributed to conceptualization, methodology, investigation, formal analysis, and resources, while also leading visualization and validation efforts and refining the manuscript through review and editing. **Seyed Mohammad Azimi** supported project administration and supervision, contributed to investigation and formal analysis, and assisted in manuscript review and editing. **Peyman Bayat** contributed to visualization, validation, resources, investigation, and formal analysis, and participated in manuscript review and editing.

DATA AVAILABILITY

All data produced or examined in the course of this study are fully contained within this published article.

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