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Design and simulation of optical logic gates based on insulator - metal – insulator (IMI) plasmonic waveguides for optical communications

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Abstract

In this study, a structure has been proposed implementing the optical Plasmonic logic gates (OR, NOR, AND, NAND, NOT) using the linear Plasmonic waveguide and the double ring resonator. The results of these gates were analyzed and simulated by means of Comsol Multiphysics (5.6) using Finite Element Analysis (2-FEM). These gates were implemented in the same structure depending on the characteristic of constructive and destructive optical interference between the signals propagating in the input ports and the control port, the phase and direction of those signals, as well as the positions of these ports. Hence, the performance of these gates was measured according to two criteria, first, the optical transmission ratio and the second, the contrast ratio, which is the ratio between the transmitter ON state of logic (1) and OFF for logic (0).

Keywords: Optical logic gates, Plasmonic waveguide (IMI), surface plasmon polarization (SSP)

1. Introduction

Scientific research on Plasmonics started in early 1902 by R.M. Wood when he noticed a dark band in the light spectrum emitted from a metal grating, which is now called Wood's anomaly [18]. Later in 1907 a physical explanation for the phenomenon was proposed for Lord Rayleigh phenomenon [25]

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of the anomaly occurring in the diffracted light spectrum at a wavelength from which an accidentally scattered wave emerges on the surface. Two decades later, Ugo Fano predicted the semi-stationary polarized waves that resonate along the metal surface. This loss of energy is due to cohesion when exciting the electrons in the metal, which were later called surface plasmons [7]. In 1968, Erich Kretschmann [11] and Andreas Otto [23] began almost simultaneously studying the methodology of surface plasmons. The optical devices based on (SPPs) have become of interest to researchers in recent years, because the need for high bandwidth and high speed for data transmission had increased. SPPS devices overcome the main limitations of electronic devices, such as delay in data transmission speed and high heat generation. (SPPS) also help overcome the diffraction limit in traditional optical devices and light processing on the sub-wavelength scale. This feature encouraged shifting attention to micro guiding structures which confine sub-wavelength light. Plasmonic waveguides showed good potential in guiding light patterns of sub-wavelength, since (spps) is the interaction of electromagnetic waves and free electrons of metals that propagate on metal-insulating or insulating-metal interfaces [30, 27]. So far, a variety of Plasmonic waveguiding structures have been proposed, for example filters [24] grooves [2] nanowires [6] nanocavities [31] stub waveguides [9] Bragg reflectors [31] resonators [8] comparisons [21] modulators [14] multi/demultiplexers [20] switches [29] logic gates [13, 17]. In case of logic gates, many studies have been proposed and analyzed, for example Semiconductor single photonic amplifiers [10], two-photon absorption in silicon waveguides [22], two-cavity photonic hybrid nanobeam [17], and silicon micro-resonator [33].
The second part of the current study explains the related previous work. The third part explains the theoretical and dimensional calculations for this proposed structure. The fourth part explains the practical results and simulations for all the proposed gates. The last part is a summary of this research where the results of simulations are discussed.

2. Literature Review

In [4], a structure was proposed to implement the optical Plasmonic logic gates (NAND, NOT, EX-OR and EX-NOR) based on the Plasmonic waveguide and the nano-sized disc resonator. The geometric dimensions of the structure are (1220×1120) nm. The highest contrast ratio in this structure is 26db, and the applied wavelength is 525 nm. These gates were simulated and studied using the FDTD method. The best performance was for the XOR gate in this structure.
A structure is proposed in [1] to implement (XOR, OR, AND) gates, based on coupling (SSPs) between graphene nanoribbons spatially separated with silica (SiO2) separated by a distance that allows the effective coupling between the Plasmonic modes of waveguides. It was numerically analyzed for the behavior of (SPPs) propagation in the interferometer as a function of chemical potential and engineering parameters in order to obtain the logic gates mentioned to apply OOK.
A structure to implement an optical Plasmonic NOT logic gate based on the Plasmonic waveguide (MIM) was proposed in [32]. All the proposed gates have been numerically studied using the Finite Difference Time Domain (FDTD) method, and the optical NOT logic gate was implemented by changing the control port state. To decide whether the outgoing field propagate in the waveguide or not. Small nano-ring (MIM) Plasmonic waveguides were used with the size of the proposed structure being as relatively large as $(2.4\mu m \times 3\mu m)$ and the maximum transmission was 65.35 in this structure.
An optical Plasmonic logic gates (XOR, XNOR) have been proposed based on different resonators in [19], which are Plasmonic ring resonators (PRRs), metal-insulator-metal (MIM) and octagonal rings. All the proposed gates were numerically studied using the two-dimensional finite difference time domain method (2D-FDTD), where the performance of the gates was measured through the variance property. The results were $(22.66-22.9)$ db for the gates (XOR, XNOR) when the resonator

was square and tge contrast ratios were db $(23.01 - 23.53)$ when the resonator was octagonal for the gates (XOR, XNOR).

In [20], optical Plasmonic logic gates (NOT, AND and NOR) were proposed implemented in two structures. They were based on the structures of Plasmonic waveguides (MIM) and the square ring resonator. The geometric dimension of the first structure was ($750nm\ x900nm$) to implement the NOT gate, and the geometric dimension of the second proposed structure was ($1.5\mu m\ x1.8\mu m$) for both AND and NOR gates, where the highest transmission ratio for both structures was 70% and 90%, respectively. The applied wavelength of these gates was 1535 nm.

In [4], photoplasmic (MIM)-based (EX-OR, OR, NOT) gates were proposed with a slot cavity resonator, with geometric dimensions of this structure as $(760 * 600)$ nm. All proposed gates were analyzed numerically by (FDTD) method, and the highest contrast ratio was 26 db.

In [26], a structure implementing optical Plasmonic logic gates (AND, XNOR, NOR) was proposed, based on metal-insulator-metal graphene. The structure contains one input port and three output ports. The dimensions of the proposed structure were $4.5\mu m$, the width of the SiO2 layer = 120 nm, the width of the Au layer = 30 nm, and the thickness of the graphene layer is one atom. The highest contrast ratio obtained is (29.41, 97.38 and 29.40 db in AND, XNOR, NOR gates), respectively.

In [28], a structure implementing the NAND gate was proposed, based on Mach-Zehnder of Plasmonic interferometer (P-MZI) and MIM waveguides. The lowest number of P-MZI was used in the proposed structure, operating at wavelength 1550 nm. The geometric dimension of the proposed structure was ($40x7.5\mu m$) and the highest contrast ratio in this gate was 10.25 db.

In [34], OR, NOT, AND, and EX-OR logic gates were proposed, based on a matrix waveguide. The structure contains one input port and three output ports. The waveguide length (L) is changed to get the gate to be implemented of the proposed gates. Hence, when $L1 = 0.68\mu m$ it is for an NOT gate, when $L2 = 0.38\mu m$ it is for an AND gate and when $L3 = 0.32\mu m$ it for an XOR gate. On the other hand, the highest contrast ratio obtained is db 13.98. The logic functions of OR, AND, NO and XOR gates can be implemented by choosing the appropriate waveguide length, specifying the input and output ports and the appropriate transmitting threshold value where the waveguide lengths of the proposed gates differ.

In [12], a structure was built to implement optical Plasmonic logic gates (AND, NOR) based on waveguides and a circular resonator (MIM). The highest transmission rate obtained in this structure was in the AND gate, which was 84.06%.

In [5], the optical Plasmonic logic gates (XOR, OR and NOT) were proposed, based on graphene nanoribbon resonators of precisely designed structures of nano-waveguides as ports for logic input and output. The results were verified numerically using (FDTD) method. The highest variance ratio (8db) was obtained between the logical states ON and OFF, based on the good feature of the chemical potentials of graphene conduction. Its behavior and performance can be effectively controlled by manipulating the properties of the structures.

In [16], a structure implements optical Plasmonic speech gates OR and NOR was proposed based on the proposed linear waveguides and vertical linear cavities that use MIM Plasmonic structures with a high contrast ratio. $(W) = 50$ nm. The length of the vertical linear cavity (L) was 1000 nm, and the highest contrast ratio was obtained in the NOR gate of about (12.36 db).

These previous studies aimed to reduce the size of the optical devices used in communication systems. Most of these studies implemented a few optical gates of the same structures implementing a number of gates in one structure or more. Also, some previous studies changed some dimensions of the same structure to implement another gate. In the current study, five optical gates were implemented, which means a large number of gates in the same structure, the same transmission threshold, and the same wavelength of 1550 nm. It is hoped that this study will be a gateway to build photonic

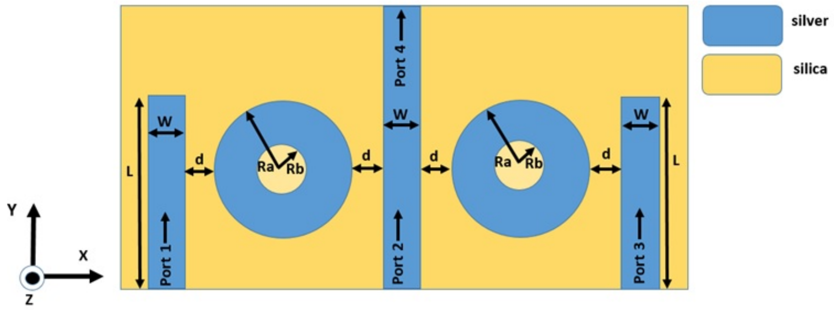


Figure 1: Proposed installation to implement optical-Plasmonic logic gates

Plasmonic integrated circuits.

3. Theoretical Calculations and Proposed Structure

In the current design, a structure is proposed and simulated implementing Plasmonic optical gates (OR, NOR, AND, NAND, NOT) using Plasmonic technology. The proposed structure to implement these gates is shown in Figure 1. It consists of three linear nano-waveguides and two double-loop resonators based on Plasmonic waveguides (insulator-metal-insulator) (IMI) to implement the proposed gates. The dimensions are (200∗400) nm, the length of the middle waveguide and the side waveguides are (200,150) nm, respectively, and the width of the linear waveguides (W), is (35) nm. The inner and outer radius of the resonator (Ra, Rb), are (70,10) nm, respectively. As for the distance between the linear waveguides and toroidal resonators (d), it is (2.5) nm. The materials used in the proposed structure are silver and silica. The linear waveguides and ring resonators are of silver and the rest of the structure is silica as shown in Figure 1. All the proposed gates in the structure have the same dimensions, the same parameters and the same materials in the same structure. In our simulation, Johnson and Christie data were used to describe the permittivity of silver and the refractive effect of the insulating material was (1.44). The refractive effect coefficient of the material, the dimensions of the structure and the materials used in the structure are the basis the resonance wavelengths of the Plasmonic systems. The resonant wavelength can be calculated by equation (3.1) [20].

$$\lambda_m = 4\pi n_{eff} D/m \tag{3.1}$$

Where n_{eff} is the refractive effect index and D is the large diameter of the nano-ring resonator according to equation (3.1). A resonant wavelength was used in the current research which is 1550 nm because many optical systems use this wavelength in their applications.
Whereas, in refs. [15] the scattering relationship in the TM waveguides can be calculated by.

$$\varepsilon_m k_d + \varepsilon_d k_m tanh\left(\frac{k_m}{2} w\right) = 0 \tag{3.2}$$

Where: (ε_m) is the dielectric constant of metal
(ε_d) is the dielectric constant of insulator
(w) is the thickness of metal k_d and k_m are obtained by:

$$k_d = (\beta^2 - \varepsilon_d k_o^2)^{\frac{1}{2}} \qquad \textit{Dielectric wave number} \tag{3.3}$$

$$k_m = (\beta^2 - \varepsilon_m k_o^2)^{\frac{1}{2}} \qquad \mathit{Metal\ wave\ number} \tag{3.4}$$

Where ε_d and ε_m are dielectric constants of the insulator and metal.

$$k_o = \frac{2\pi}{\lambda} \qquad \mathit{Free\ space\ wavenumber} \tag{3.5}$$

(β) is the propagation constant which can be represented by the refractive effect n_{eff} as in the equation:

$n_{eff} = \frac{\beta}{k_o}$

The proposed installation in the current study has four ports, two of which are considered as input ports, the third port is control, and the fourth port is an output port. The required port behavior can be obtained in the output port by activating the input ports and the control port and tuning them together. The performance of each optical Plasmonic gates can be measured through two criteria, the first is the transmission of optical power from the input ports and the control port to the output port as a function of wavelength. This can be achieved by choosing a threshold value for the transmission between logic (1) ON state and logic (0) OFF state at the output to determine the in the ON or OFF state. The same transmission threshold has been chosen for all the optical gates proposed in this installation to be 30%. The second criterion is the contrast or extinction ratio, which is the ratio between the transmission or the optical power of the ON and OFF states in the output port, where the contrast ratio of the optical output power or transmission The greater the performance, the better the performance of the Plasmonic logic gate, as these two criteria are described in Eqs. (3.6) [32] and (3.7) [4].

$$T = P_{out/}P_{in} \quad (\mathit{for\ the\ ON\ and\ OFF\ states\ in\ the\ output}) \tag{3.6}$$

T is the transmission, P_{out} represents the optical output power at the output port in the ON and OFF states, P_{in} represents the optical input power to the input ports and the control port

$$^{ON}/_{OFF}\ \mathit{contrast\ ratio}(db) = 10\log_{10}[(P_{out}|on)_{\min}/(P_{out}|off)_{\max}] \tag{3.7}$$

Where

$$P_{out}|ON\ \mathit{is\ the\ optical\ power\ at\ the\ output\ port\ in\ the\ ON\ state},\ logic(1)$$
$$P_{out}|OFF\ \mathit{is\ the\ optical\ power\ at\ the\ output\ port\ in\ the\ OFF\ state},\ logic(2)$$

The transmission of optical power from the input ports and the control port to the output port in the ON state logic (1) is given the symbol T_{ON}, which means that T_{ON} is higher than 30% for all ON states in the proposed Plasmonic logic gates. The output port is in the OFF state. Logic (0) is denoted by the symbol T_{OFF}, which means that T_{OFF} is less than 30% for all OFF states in the proposed Plasmonic gates, so the equation (3.7) will be as follows.

$$^{ON}/_{OFF}\ \mathit{contrast\ ratio}(db) = 10\log_{10}[(P_{out}|on)_{\min}/(P_{out}|off)_{\max}] = 10\log_{10}(\frac{T_{ON}}{T_{OFF}}) \tag{3.8}$$

The transmission of optical power will be higher or lower depending on the shape, size and parameters of the proposed structure, materials, refractive effect of the selected materials, locations

of the ports, polarization and phase of the applied field.
The interaction between the linear waveguides and the nano-double-loop resonators that will form a new surface Plasmonic resonance that comes as a result of coupling the linear waveguides with the double-loop resonators and the paired Plasmonic waves are strong depending on the near field at very short distances. The coupling distance (d) must be small for the continuation of this process and to obtain the highest improvement in the field. If the coupling distance increases, the transmission spectrum and field will decrease. Based on the current work and the results obtained, the best coupling distance between the linear waveguides and the double-loop resonator is (2.5) nm.
In order to achieve constructive interferences, the phase and direction of propagation of the signals going into the input ports and the control port have to be similar. Otherwise, to achieve destructive interferences, the phase or propagation direction of the waves going into the ports should be different. The order of interference (m) is described by the following modifier in Eqs (3.9) [3].

$$m = \frac{4n_{eff} d \cos\theta}{\lambda} \tag{3.9}$$

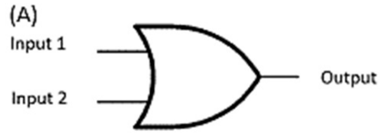
where (m) is the interference order, (n_{eff}) is the refractive effect of the dielectric material, (d) is the thickness of the metal material, (θ) is the phase angle of the applied or input signal, (λ) is the applied wavelength.
(θ) here plays a significant role in determining the transmitted optical power (T, where at $\theta = 0$, the interference order (m) in equation (3.9) is positive. This means that it will be constructive interference and that the transmission (T) will increase and when it is $\theta = 90$ the interference rank (m) in equation (3.9) will be zero and no interference will occur. This means that the phase of the applied signal does not affect the optical transmission power and the transmission (T) will increase or decrease depending on other parameters whereas when $\theta = 180$, the interference order (m) in equation (3.9) will be negative. This means that the direction of propagation of the current pattern is opposite to the directions of other propagation in the other ports. Consequently, this leads to destructive interactions between the signals propagated in the different ports as a result of the phase difference of the applied signals, hence, the light transmission (T) will decrease.

4. Results and Simulations

4.1. Optical-Plasmonic OR logic gate

Based on the discussion in the theoretical part, the implementation of OR gate by the current proposed structure is operated by making port (1) and port (2) input ports, port (3) a control port and port (4) an output port, as in the figure 3. And through the fact table of the logical OR gate in the figure and its structure shown in Figure 2 it can work as an OR gate where the function of this gate is achieved through constructive interferences occuring among the light signals scattered in the input ports in and the control port, since in this gate we do not need to change the phase between the input ports and the control port in order to obtain the highest transmission rate for most cases in this gate. When the two inputs are ON, the interference will be constructive, because the optical signal propagated in the three ports, the input port and the control port, are all in the same phase and direction of propagation, the transmit signal will be doubled, and the output in this case in port (4) is ON. When only one of the input ports is ON, there will also be constructive interactions between the input port and the control port, and the output in port (4) will be ON as well, but when the two input ports are OFF, there will not occur any interference condition only occurs, instead the transmitter signal will be weak because it will be from one port only, which is the control port. So the output in port (4) is OFF. Figure 4 shows the transmission spectrum of the OR gate, and Figure 5 shows the distribution of the electric field on the Y-vehicle for all the states of this gate.

(A)



(B)

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Figure 2: (A) OR logic gate symbol (B) OR gate fact table

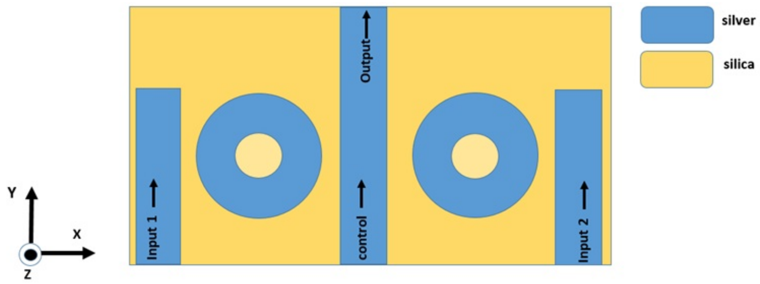


Figure 3: Proposed structure for implementing an optical Plasmonic OR logic gate

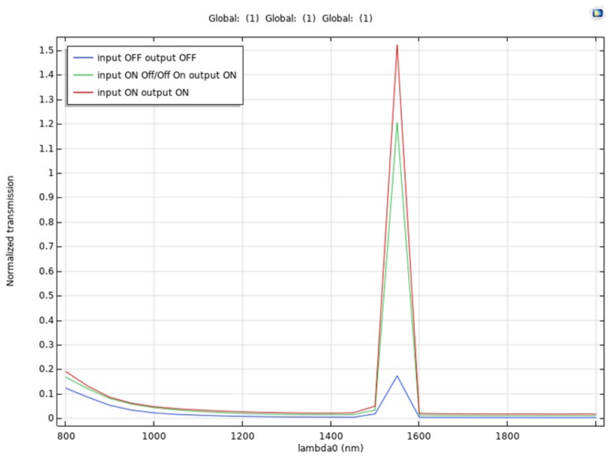


Figure 4: Illustrating the transmission spectrum that shows the relationship between the transmission and the wavelength of all states of the optical Plasmonic OR logic gate

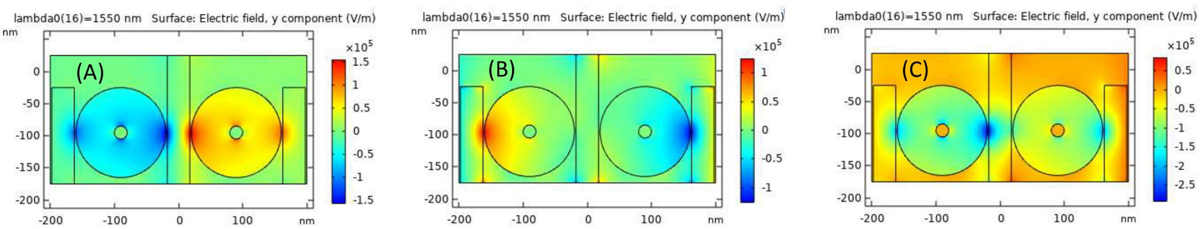
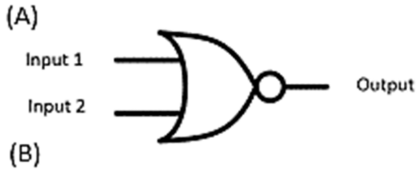


Figure 5: The distribution of the electric field on the Y vehicle. (A) When the two inputs are OFF (B) When the two inputs are ON (C) When only the first or second input is ON



(B)

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 6: (A) NOR logic gate symbol (B) NOR gate fact table

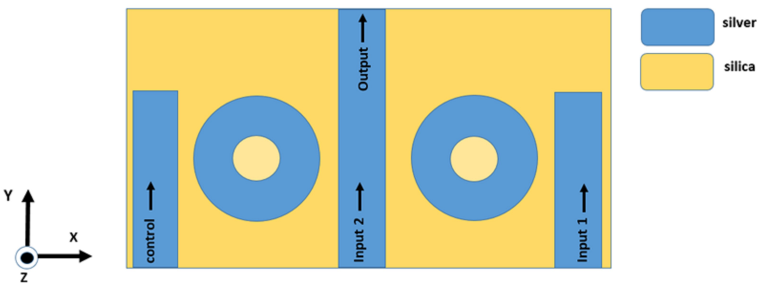


Figure 7: Proposed structure for implementing an optical Plasmonic NOR logic gate

4.2. Optical Plasmonic NOR gate

To implement the NOR gate in the proposed structure, the two input ports are port (2) and port (3), and port (1) is the control which is placed here to weaken the transmitter because most of the solutions for this gate must be OFF. And port (4) is made as an output port as shown in Figure 7 where through the truth table of the logical NOR gate in the figure and its shape shown in Figure 6 it can work as a NOR gate where the function of this gate can be achieved through the destructive interferences that occur between the light signals scattered in the input ports and the control port. When the two input ports are OFF and the control port is ON, the output in port (4) will be ON. When one of the input ports is ON, the output in port (4) will be OFF, but in the latter case of this gate, when the two input ports are ON and the phase angle of the first input into port (3) is zero (0°) and the phase angle of the second input in port (2) is (90°) degrees, in this case, there will be a phase difference between the light signals in the input ports and the control port. The interference will be destructive and the output in port (4) is OFF. Figure 8 shows the transmission spectrum of the NOR gate, and figure 9 shows the distribution of the electric field on the Y- vehicle for all states of this gate.

4.3. Optical Plasmonic AND logic gate

To implement the AND gate by the proposed structure, the two port (1) and port (3) are made input ports and port (4) is made control. The signal propagation of this port opposite is to the direction of the signal propagation of the input ports, which leads to weakening the transmission according to the out ports of the logical AND gate where most of its output ports states are OFF. Port (2) will be considered an output port as shown in Figure 11. The fact table of the logical AND gate in the figure and its structure are shown in Figure 10 an AND gate can be made. The function of this gate is done through the destructive and constructive interferences occur between the optical

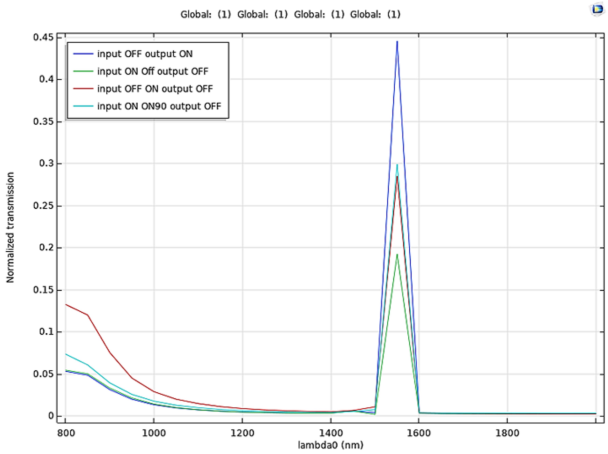


Figure 8: Illustrating the transmission spectrum that shows the relationship between the transmission and the wavelength of all states of the optical Plasmonic NOR logic gate

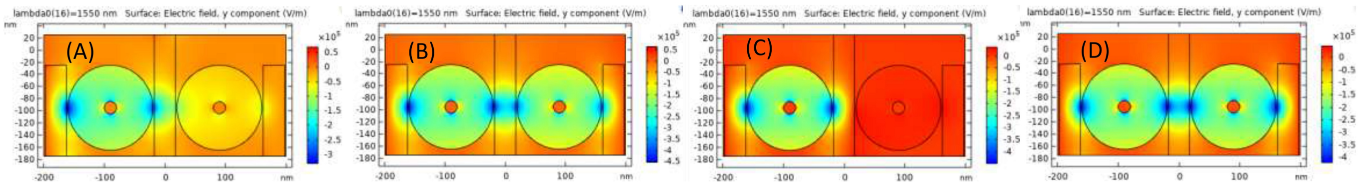
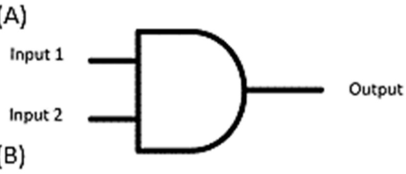


Figure 9: Showing the electric field distribution on the Y vehicle. (A) When the two inputs are OFF (B) When the two inputs are ON (C) When only the first input is ON (D) When only the second input is ON

signals scattered in the input ports and the control port resulting from the phase difference and the direction of propagation of the optical signals applied to these ports and output in port (2) is ON. In the case when either of the two inputs is in the ON state and its phase angle is (180°) degrees, destructive interference will occur due to the phase difference and the direction of propagation of the input signals and the control signal, then the output in this case in the output port (2) is OFF. But in the case when both input ports are OFF, the transmission will be weak and the output in port (2) is OFF. Where the figure 12 will show the transmission spectrum of the AND gate, and the figure 13 shows us the distribution of the electric field on the Y component for all states of this gate.

(A)



(B)

Input 1	Input 2	output
0	0	0
0	1	0
1	0	0
1	1	1

Figure 10: (A) AND logic gate symbol (B) AND gate fact table

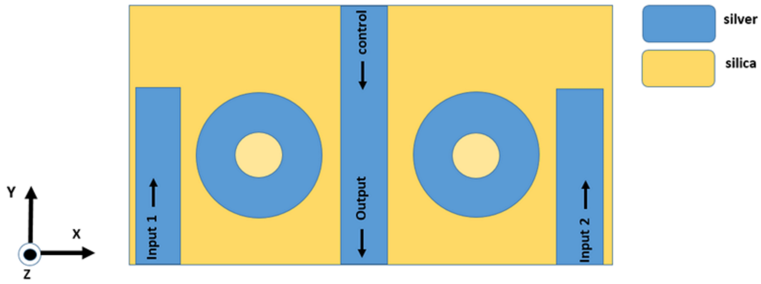


Figure 11: Proposed structure for implementing an optical Plasmonic AND logic gate

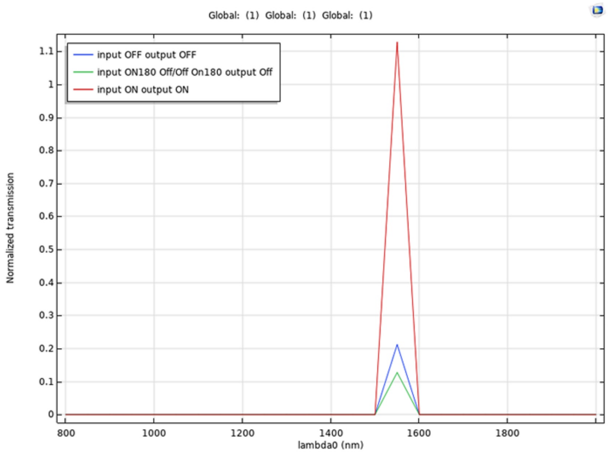


Figure 12: Illustrating the transmission spectrum that shows the relationship between the transmission and the wavelength of all states of the optical Plasmonic AND logic gate

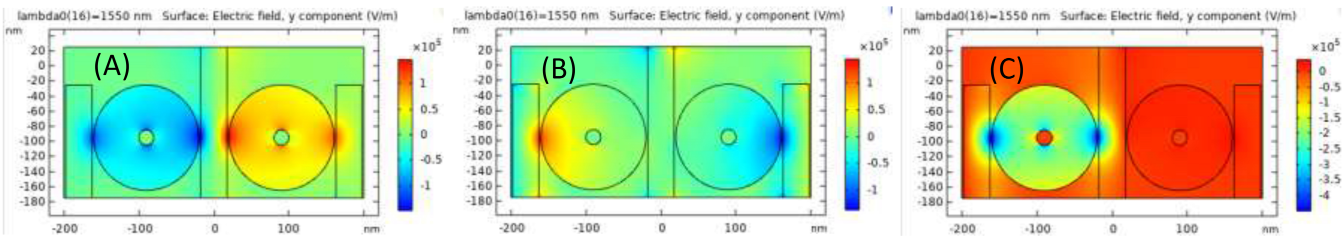
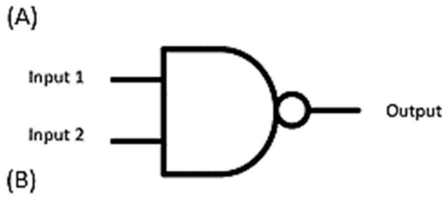


Figure 13: Showing the electric field distribution on the Y vehicle. (A) When the two inputs are OFF (B) When the two inputs are ON (C) When only the first or second input is ON



(B)

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 14: (A) NAND logic gate symbol (B) NAND gate fact tab

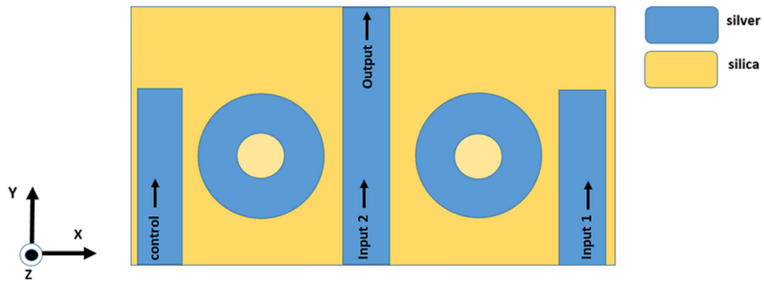


Figure 15: Proposed structure for implementing an optical Plasmonic NAND logic gate

4.4. Optical-plasma NAND logic gate

To implement the NAND gate by the proposed structure shown in Figure (1),port (2) and port (3) are made input, port (1) is made control and port (4) is made output port as in Figure 15. The fact table of the logical NAND gate in the figure and its structure are shown in Figure 14. It can work as a NAND gate. The function of this gate is done through destructive and constructive interferences that occur among the optical signals scattered in the input ports and the control port resulting from the phase difference of the optical signals propagated through these ports. When the two input ports are OFF and the control port is ON, there will be no constructive or destructive interference and the output in port (4) will be ON because the transmission value will be higher of the transmission threshold which is 30%. When any of the input ports is in the ON state, constructive interference will occur between the optical signals in the input ports and the control port, which is always ON. In these cases, the output in port (4) will be ON, but in the case when the two input ports are ON, the phase angle of the first input into port (3) is (180°) and the phase angle of the second input into port (2) is (90°), there will be a phase difference Between the optical signals scattered in the input and control ports, destructive interference will occur due to the phase difference, and the output in this case in the output port (4) will be OFF. Figure 16 shows the transmission spectrum of the NAND gate, and figure 17 shows the distribution of the electric field on the Y-vehicle for all states of this gate.

4.5. 5 Optical Plasmonic NOT logic gate

The NOT gate is the last to be implemented in the proposed structure. Port (2) is made input where one port is used for input into this gate because there are only two states; either ON or OFF. Port (1) is the control port and port (4) is the output, and port (3) was neglected by making it OFF

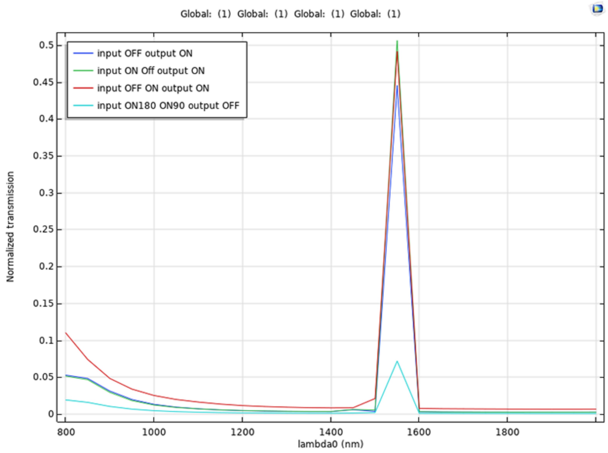


Figure 16: Illustrating the transmission spectrum that shows the relationship between the transmission and the wavelength of all states of the optical Plasmonic NAND logic gate

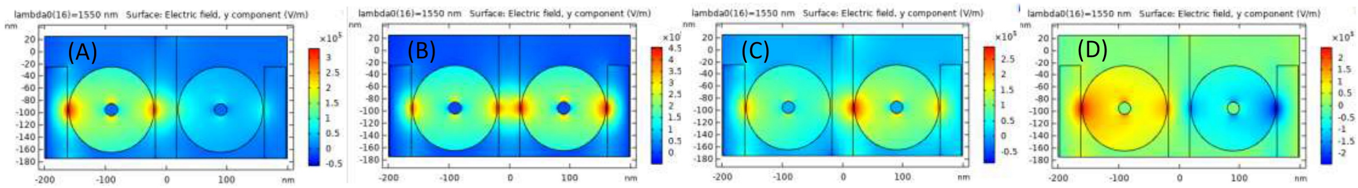
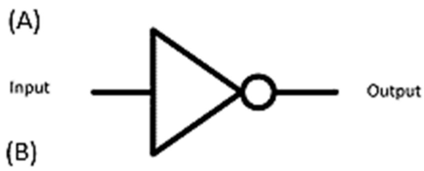


Figure 17: Showing the electric field distribution on the Y vehicle. (A) When the two inputs are OFF (B) When the two inputs are ON (C) When only the first input is ON (D) When only the second input is ON

for all gate states. The structure is shown in Figure 19, the fact table of the logic NOT gate in the figure and its structure are shown in Figure 18, it can work as a NOT gate. To achieve the function of this gate, this is done by destructive and constructive interferences that occur between the light signals defused in the input port and control port. When the input port (2) is ON and the control port is also ON, the output in port (4) will be OFF, but when the input is OFF and the control port is ON, the output in port (4) will be ON. Figure 19 shows the transmission spectrum of the NOT gate, and figure 20 shows the distribution of the electric field on the Y vehicle for all states of this gate.



(B)

Input	Output
0	1
1	0

Figure 18: (A) NOT logic gate symbol (B) NOT gate fact table

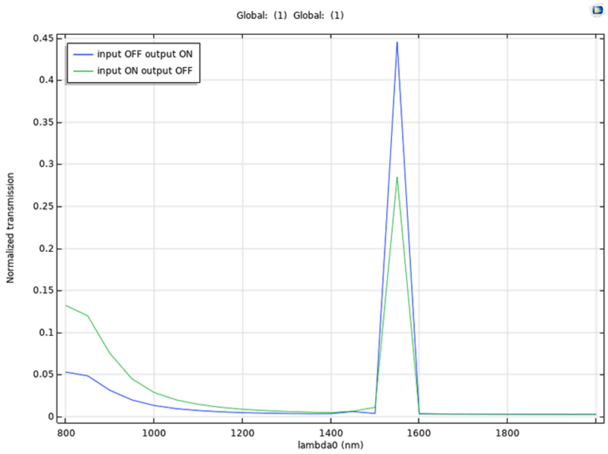


Figure 19: Proposed structure for implementing an optical Plasmonic NOT logic gate

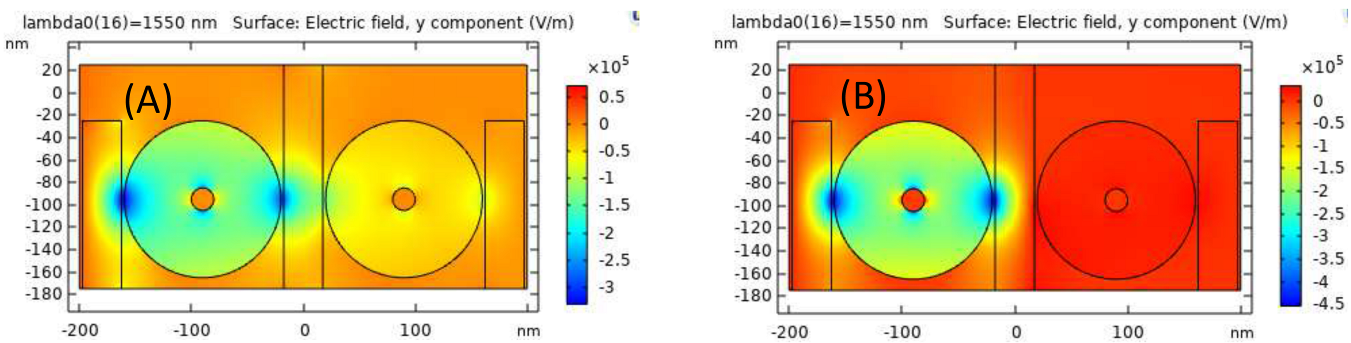


Figure 20: Showing the distribution of the electric field on the Y vehicle. (A) When the input is OFF (B) When the input is ON

5. Conclusion

In this study, a structure has been proposed implementing the Plasmonic logic gates (OR, NOR, AND, NAND, NOT) with the same structure, the same wavelength of 1550 nm and the same transmission threshold 30%. These proposed gates were achieved through the property of coupling between linear Plasmonic waveguides and (IMI) double-loop resonator where these gates can be implemented by changing the state of the inputs, the positions of the input and control ports and the phase of the signal applied in those ports. The transmission in the output port can be made as higher or lower as possible according to the required gate and its own fact table by changing the coupling distance (d). The best coupling distance used in the current study is (2.5) nanometers. The results obtained by simulations, some gates transmission rate obtained were higher than 100%, such as the OR gate, where the highest transmission rate was 152%, as well as in the AND gate, the highest transmission rate was 112%.

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