Design and Experimental Verification of a Single-Phase Multi-Level Asymmetric Inverter

Bahman Taheri, Asghar Akbari Foroud*

***Abstract*— Inverters have evolved significantly in the last decade as a key component in electrical systems. Improving the performance of the inverters is a challenge, leading to many types of researches on topologies and control schemes. Multi-level voltage source inverters are suitable structures to achieve high-power and high-quality output waveforms. Till now, wide studies have been conducted in the field of multi-level inverters used in high-power and voltage applications, which have attracted attention due to their advantages, including less harmonic distortion of output waveforms, less tension of switch voltages, and low electromagnetic interference. In this paper, a sinusoidal pulse width modulation (SPWM) cascade full-bridge single-phase 7-level inverter with phase shift modulation is designed using a suitable voltage control with low capacitance for asymmetric condition and its performance is investigated. The performance of the proposed inverter is investigated under different operational conditions through simulations in MATLAB. Besides, for more investigation, an experimental sample of this inverter is constructed and the practical results are presented. The experimental results show that the output harmonic current of the inverter under symmetric performance of the output current is 1.51%. Although this THD is higher than the value obtained in the simulation results, it complies with the ISIRI 11859 standards for the current THD, which indicates that a THD less than 5% is acceptable.**

Keywords: cascade full-bridge inverter, harmonic distortion, modulation, photovoltaic

1- Introduction

In recent years, multi-level inverters have emerged as a feasible power conversion solution for medium and high-power applications due to the ability to operate at high voltage/power and better harmonic performance than traditional two-level inverters. Since the output level of the multi-level inverters depends on the number of the switching elements, when more levels are used, more switching elements are required. Many multi-level converter topologies and various control methods have been developed in recent studies [1–3]. Three different basic multi-level converter topologies are commonly used, including the neutral point diode clamped (NPC), flying capacitor (FC), and the cascaded H-bridge (CHB) [4, 5]. In [6-8], a novel structure has been proposed for multi-level inverters, which is called type “T” inverter. This structure employs the structure proposed in [6] and extracts a single-phase 5-level inverter. Among the main features of this structure, a significant reduction of power elements compared to conventional structures can be mentioned. Another multi-level inverter has been proposed in [9]. This structure requires double-sided switches to connect and disconnect paths to obtain different levels. This structure requires fewer drivers (equal to the number of double-sided switches), reducing circuit complexity. In [10-11], a topology has been proposed for multi-level inverters in which switches are put in series with sources and reduced elements. In [12], a detailed survey is made on the recently designed multi-level inverter to find the suitability of the inverters for particular applications. Research is performed on various types of multi-level inverters such as symmetric, asymmetric, hybrid and modularized multi-level inverter to identify the issues in generating more levels at the output. A summary of various issues in multi-level inverter with reduced switch count is provided so that a novel topology of the multi-level inverter can be designed in future. In [13], a novel structure has been proposed for multi-level inverters with asymmetric switching. In this reference, a new inverter model has been proposed based on the switching function model in order to calculate analytical relationships of harmonics for asymmetric switching. In [14], a novel symmetric multi-level inverter structure based on independent DC voltage sources has been proposed, which has fewer devices than other devices, reducing the complexity of its control system and driver circuits. The proposed structure is a comprehensive structure, which can be easily extended to an arbitrary number of voltage levels. In [15], a single-phase asymmetric hybrid multi-level inverter has been proposed by combining diode clamped and cascaded H-bridge topologies. The authors of [16] have introduced a new multi-level converter topology, which can supply bidirectional current loads. The proposed structure has fewer power electronic devices such as power switches, driver circuits, power diodes, and DC voltage sources Furthermore, it can be designed in symmetric and asymmetric structures. A new multi-level inverter is designed to improve the power and voltage quality, containing fewer switches in the specified voltage levels. The proposed inverter includes power electronic devices such as switches and a diode and DC inputs. In the proposed structure, considering a basic cell, including a DC source, a power switch and a diode, two levels are added to the output levels of the base

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structure [17]. A new structure has been proposed in [18] for multi-level inverters with series and parallel switching capacitors which has a higher augmentation capacity than similar structures. In [19], a single-phase asymmetric hybrid multi-level inverter has been proposed by combining diode clamped and cascaded H-bridge topologies. The inputs of the proposed inverter are selected as two unequal DC voltage sources. In this regard, fewer switching elements are used to obtain the same number of voltage levels at the output, compared to traditional multi-level inverters. The efficiency and the harmonic performance of the proposed topology are verified through simulation and experimental studies.

The gating signals of the semiconductor switches are produced by phase disposition pulse width modulation with a carrier frequency of 4 kHz. It is shown experimentally that a maximum efficiency of 94 % and a total harmonic distortion of 29 % are attained in the case studies. The purpose is to design a hybrid generalized SC-MLI with reduced components to maintain a constant voltage across the capacitors and achieve a higher voltage gain with minimum components, minimum conducting paths, lower TSV, which is cost-effective and efficient [20]. Furthermore, in [21], a new multi-level converter topology has been introduced, which can supply bidirectional current loads.

Other researchers have proposed different structures for single-phase inverters, while the existing harmonics in output waveforms are the drawback of these works. In this paper, a new topology with phase shift modulation is proposed for multi-stage single-phase inverters to solve the mentioned problem and for removing the harmonics. Furthermore, the proposed structure has fewer power electronic devices such as power switches, driver circuits, power diodes, and DC voltage sources. Furthermore, it can be designed in symmetric and asymmetric structures. Accordingly, the contributions of this work can be summarized as follows:

1- In this paper, an SPWM cascade full-bridge single-phase 7-level inverter with phase-shifting modulation and a proper capacitor voltage control algorithm for the asymmetric condition is designed, and its performance is studied.

2- Simulation results are used to study the performance of the inverter under different operating conditions.

3- an experimental sample of this inverter is built. The practical results indicate its acceptable performance, especially the harmonic components, if the inverter's output current in symmetric operation is very low.

The rest of this paper is organized as follows. Section 2 introduces the proposed controller and inverter modeling. The implementation of the modulation scheme in the simulation platform is mentioned in Section 3. Simulation studies, including harmonic measurements and formulations, are presented in Section 4. The hardware settings of the proposed model are introduced in Section 5. The performance and measured harmonics from experimental settings are also presented in this section. Finally, the conclusion is made in Section 6

II. Modelling and Control System of the Designed Inverter

One of the advantages of cascade full-bridge inverters is that they can be easily extended to a higher number of levels without changing the control system considerably. Thus, an inverter with an arbitrary number of levels is modeled here. This inverter includes PV arrays, where each array operates along with a DC-link capacitor as a supply for a full-bridge cell. Moreover, the inductance L at the output of this inverter is used to filter harmonics injected into the network. In the end, the inverter is connected to the network through a single-phase transformer. These transformers are inserted to increase the output voltage level and separate the inverter from the network's side. Since isolation is not necessary for the systems connected to the network, the transformer reinforces the output voltage.

II.I. PV Model

A PV cell is a semiconductor diode where its p-n junction is exposed to light. A PV module is a series combination of several PV cells. According to Eq. (1), PV arrays can be modeled.

$$I_{PV} = I_g - I_0\left[\exp\left(\frac{V_{PV} + R_S I_{PV}}{\eta V_T}\right) - 1\right] - \frac{V_{PV} + R_S I_{PV}}{R_P} \quad (1)$$

Where, q is the elementary charge, K_B is the Boltzmann constant, J_Ph is the photo generated current density, J_0 is the saturation current density, T is the cell temperature, n is the diode ideality factor, R_S^' is the series resistance per unit area

II.II. Concepts and Performance of the Proposed Structure

Different structures have been proposed for single-phase inverters, where each one has advantages and disadvantages. An essential problem of these inverters is the harmonics of the output voltage waveform. Three approaches are proposed to resolve these problems: a) Using harmonic filters (active, passive or a combination of both). b) Using proper switching methods like SPWM, SHE-PWM or other modulation methods. c) Using multi-level inverter structures. In the third case, multi-level structures are used to reduce harmonics of the output voltage, so that it becomes closer to a

sinusoidal waveform. But the main difference among harmonic elimination methods, switching method (second method) and multi-level method (third method) is that in the second method, as harmonics are eliminated, the amplitude of other harmonics is increased; while, in the third method, the amplitude of other harmonics is not increased and the total THD is reduced. Considering the characteristics of multi-level inverters, a novel topology is proposed for single-phase multi-level inverters. The proposed structure is shown in Figure1.

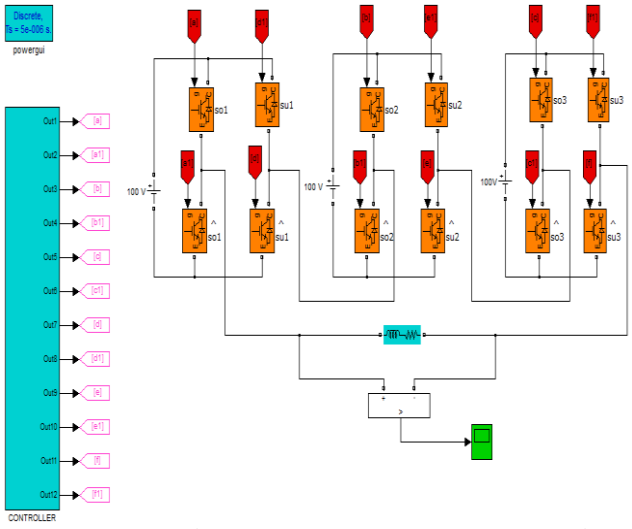

Fig (1): Schematic of the proposed 7-level inverter with phase-shifting modulation

Considering Figure.1, pulses generated for switching are generated through comparing a reference sinusoidal waveform with six triangular carrier waves with 60° phase differences, so that SPWM waveform is generated at the output. It was observed in [16] that the step angle of multi-level inverters optimized using GA are switched using phase-shift modulation at 20 kHz frequency, so that the harmonic distortion of the output voltage is reduced. Phase-shift modulation degrades and eliminates low and high order harmonics, and more harmonics are eliminated from the waveform. Figures 2 to 5 shows the FFT harmonic analysis of the inverter's output voltage with an arbitrary initial guess for different switching angles.

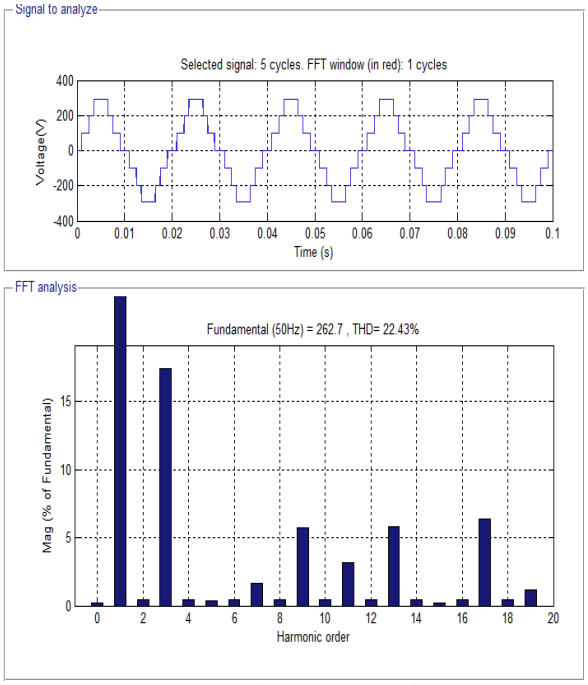

Fig (2): FFT harmonic analysis of output voltage of the inverter with initial guess of arbitrary switching angles.

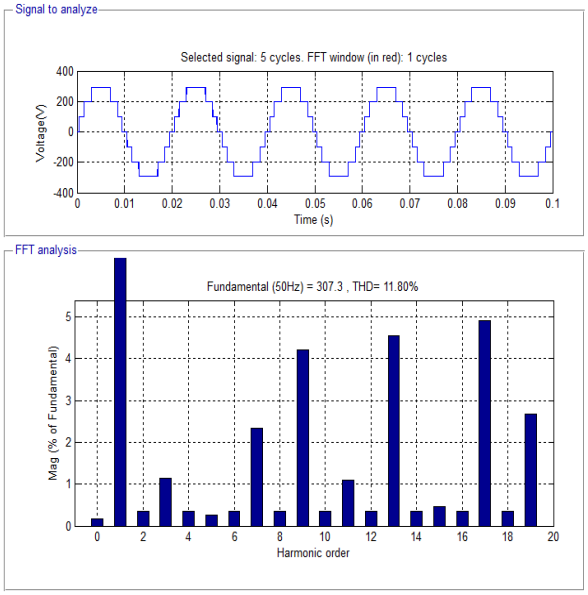

Fig (3): FFT harmonic analysis of output waveform of the inverter with optimal angles- accurate solution.

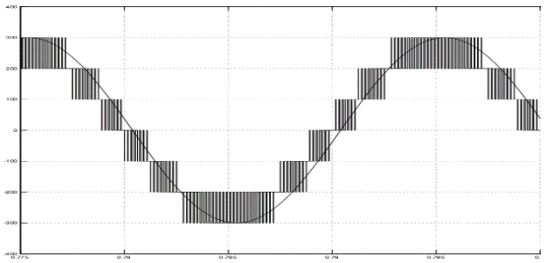

Fig (4): Output voltage waveform with M_a=0.8 and M_f=14 compared to reference sinusoidal waveform.

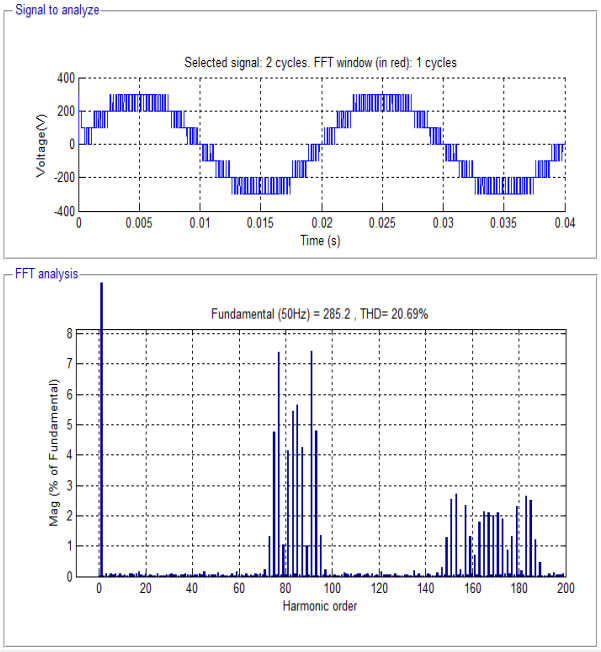

Fig (5): FFT harmonic analysis of output voltage of the 7-level inverter with amplitude modulation index of M_a=0.95.

III.The Control System

Generally, the control system should achieve the following objectives: each PV array should operate at its maximum power point to extract the maximum accessible power. The whole DC power generated by the PV arrays should be transmitted to the grid. This is done by the current injected to the grid, which should have low harmonic distortion and unit power factor. At the inverter's output, a step multi-level voltage should be generated.

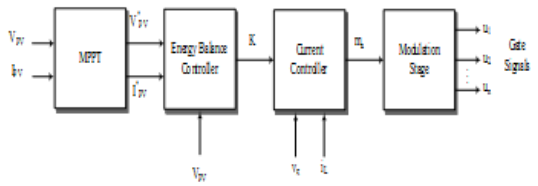

Fig (6). Block diagram of different components of a control system.

In summary, the control strategy shown in Figure 6, describes three objectives. Firstly, a proper control loop should be designed that can stabilize the voltage of the DC links using MPPT algorithm. Secondly, the desired signal for the current injected to the grid should be generated, and the output current should track the reference signal via the current control loop. The third objective is realized by the modulation stage.

IV. Simulation Results

In this section, the performance of the fuzzy control system is investigated through simulation. The characteristics of the studied system are represented in Table (1). In addition, the coefficients of the PI controller used to compensate circulating power are obtained as K_p =0.9 and K_I=10 through trial and error.

Table (1): Characteristics of the studied system.

Variable	value	unit
Capacitor of the input filter	570	µF
Inductance of the output filter	230	µH
Network frequency	50	Hz
Effective voltage of the network	110	V
Switching frequency	20	KHz
Nominal power	560	W

IV.I. Normal Operating Condition

Voltage-Power curve shows the maximum power of the PV array simulated under different irradiation levels. For the first experiment, the performance of the inverter under normal condition is investigated. After that, all three PV arrays are under an irradiation of 1000 W/ºC. Figure.6 shows the power extracted from three PV arrays from the moment being derived to a maximum power point. However, it should be mentioned that the output power of each array is passed through a low-pass filter with a cut-off frequency of 10Hz. Also, Figure.7 shows powers extracted after reaching a steady state.

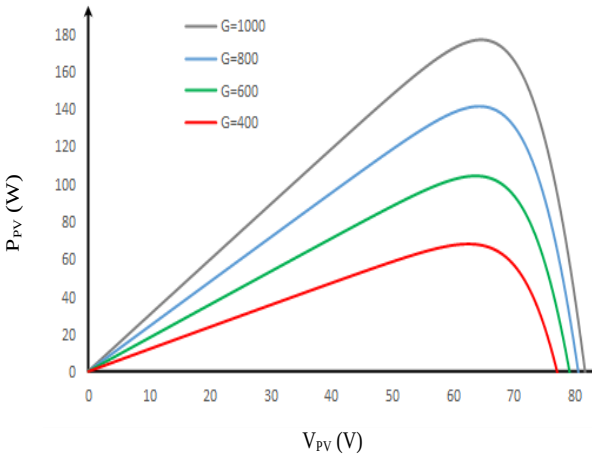

Fig (7): Voltage-Power characteristic of the PV array under different irradiation levels.

The maximum power of each array under irradiation of 1000 W/m^2 is 177.5 W. As shown in Figure 8, the control system has extracted power from each array successfully such that the output power of each array is 176.95 W.

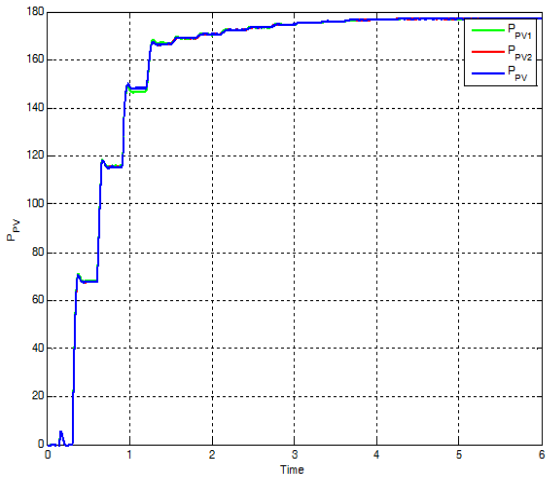

Fig (8): output power of the PV array after passing a low-pass filter under normal operating condition ($G_1 = G_2 = G_3 = 1000$ W/m^2)

According to this figure, 7-level step-sinusoidal voltage is generated at the output of the inverter, which is completely in-phase with the network voltage. Figure 10 shows the output voltage of the inverter in steady-state and the network voltage under normal operating condition (output power of the PV array after passing a low-pass filter under normal operating condition ($G_1 = G_2 = G_3 = 1000$ W/m^2)

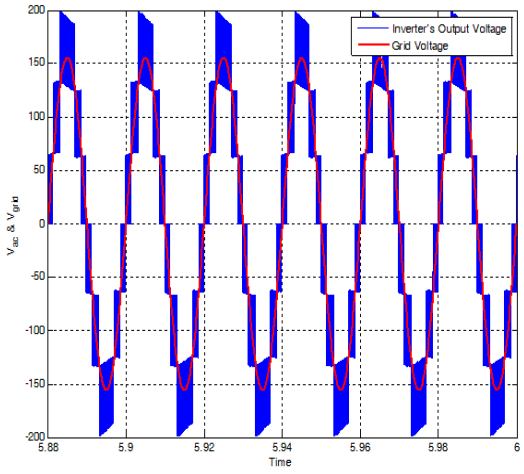

Fig (9) shows step voltage waveform of the inverter in steady state along with the network voltage. ($G_1 = G_2 = G_3 = 1000$ W/m^2)

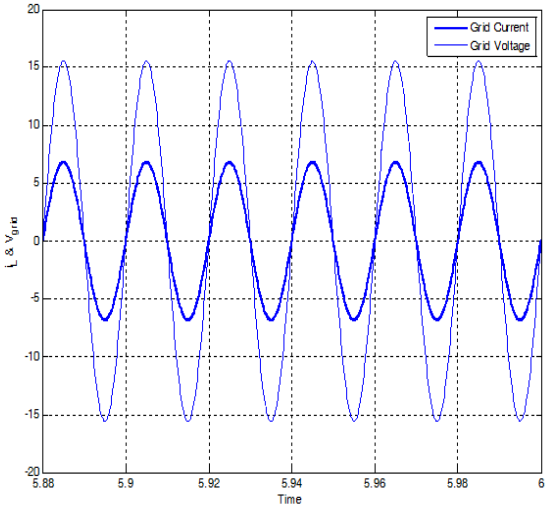

Fig (10): output current of the inverter and network voltage (coefficient of 0.1

Considering Figure 10, after 4.5s, the output power of the array reaches the maximum power. Therefore, the reference voltage is kept constant. A slight difference between the voltage of the DC link and its reference value is due to approximating the calculations of the DC link controller. In addition, since the output voltages of the three arrays are similar, only the voltage of the first array is shown.

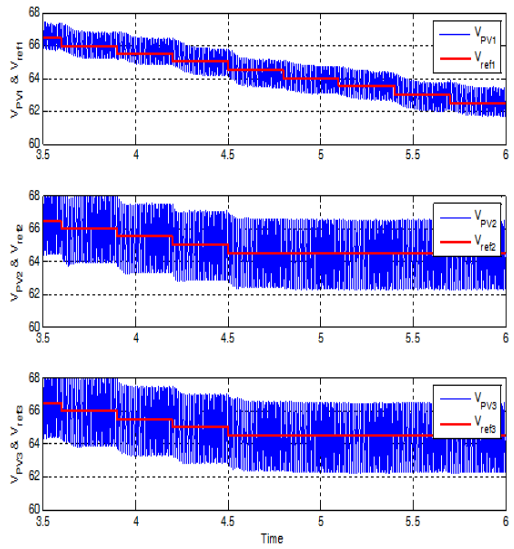

Fig (11): Voltage waveform of DC links along with their reference under asymmetric operating condition ($G_1 = 400$ & $G_2 = G_3 = 1000$ W/m^2)

The voltage waveform of DC links, along with their references, is shown in Figure 11. According to this figure, the voltage of the second and third DC links have not changed and have remained 64.5 v, while the voltage of the first DC link has reached 62.5 v. The output voltage of the inverter, and network voltage is shown in Fig.13.

According to this figure, the output of the inverter is a 7-level voltage in-phase with network voltage.

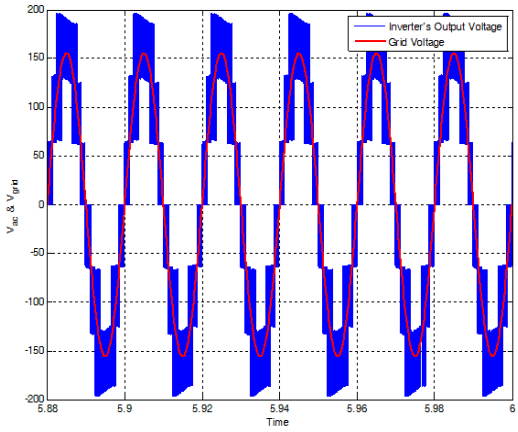

Fig (12): The output voltage of the inverter in steady state and network voltage under asymmetric operating condition (G_1 = 400 & G_2 = G_3 = 1000 W/m^2)

According to the following figure, the output current of the inverter is completely in-phase with network voltage. Considering the performance of the inverter under asymmetric operating condition (extracting power asymmetrically from all full-bridge cells), the value of the current THD has increased to 2.77%.

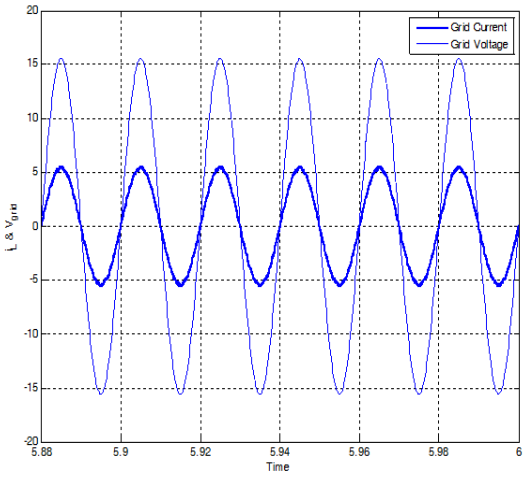

Fig (13): The output current of the inverter and network voltage under asymmetric operating condition (G_1 = 400 & G_2 = G_3 = 1000 W/m^2)

V. Implementation of the Inverter

In order to study the performance of the inverter system, an experimental sample of the cascade full-bridge 7-level inverter is implemented using a microcontroller and MOSFET. The general characteristics of the system are given in Table (2).

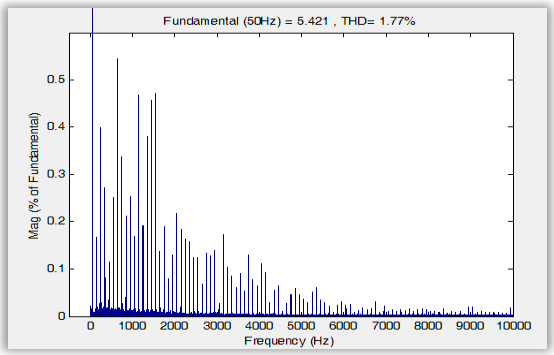

Fig (14): Harmonic component of output current of the inverter under asymmetric operating condition (G_1 = 400 & G_2 = G_3 = 1000 W/m^2)

Table (2). Characteristics of the designed system

variable	value	Unit
Capacitor of the input filter	100	µF
Inductance of the output filter	200	µH
Network frequency	50	Hz
Switching frequency	20	kHz
Nominal power	500	W

VI. Practical Implementation Results

A general schematic of the cascade full-bridge inverter connected to an ohmic-inductive load (110 ohm-10watt) is shown in fig 15.

Fig (14): Fabrication of full bridge H cell on PCB.

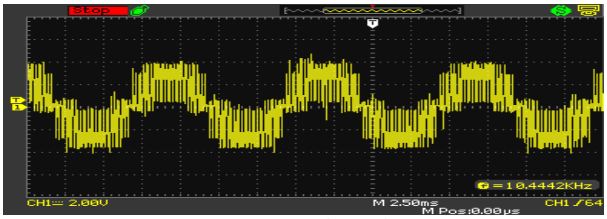

Fig (16): output voltage waveform of a 3-level inverter

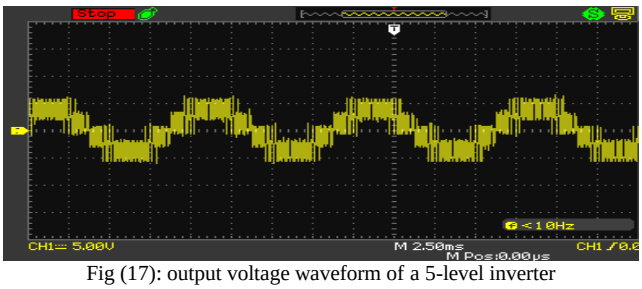

Fig (17): output voltage waveform of a 5-level inverter

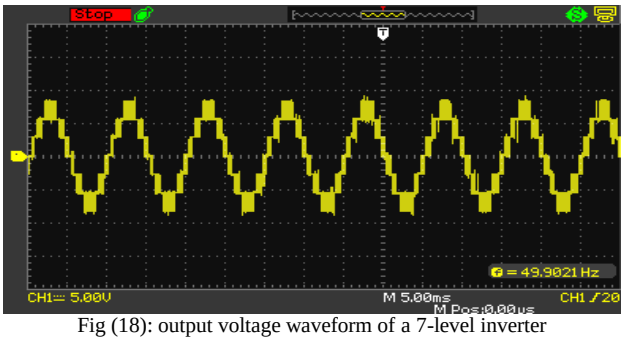

Fig (18): output voltage waveform of a 7-level inverter

Fig (19): output waveform of the inverter with SPWM modulation- 1 cycle

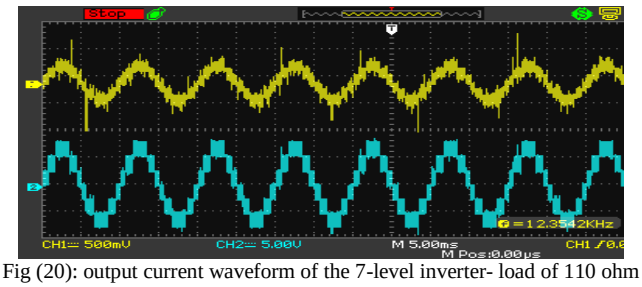

Fig (20): output current waveform of the 7-level inverter- load of 110 ohm and 200uH

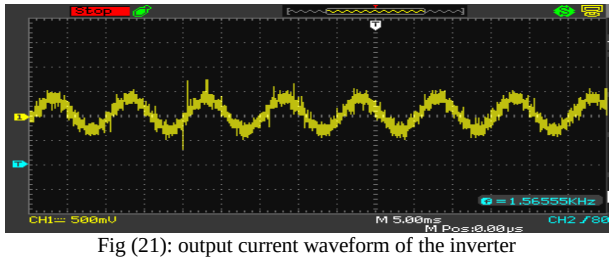

Fig (21): output current waveform of the inverter

Fig (22): output voltage waveform of the inverter along with harmonic analysis

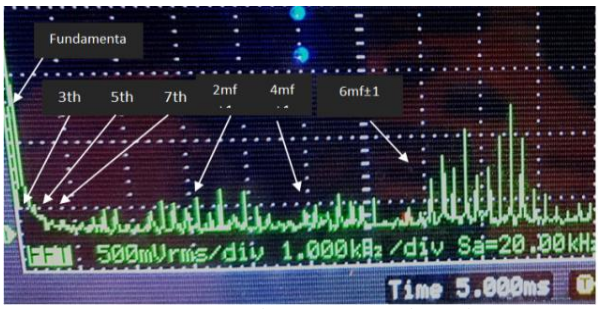

Fig (23): Harmonic analysis of the output waveform of the inverter on oscilloscope

Firstly, the performance of the inverter is studied under symmetric condition. In the experiment, each PV array is exposed to an irradiation of 1000 W/m^2. The output voltage and current waveforms of this inverter are shown in Figure 25. Mean voltage of each DC link in steady state is about 5v.

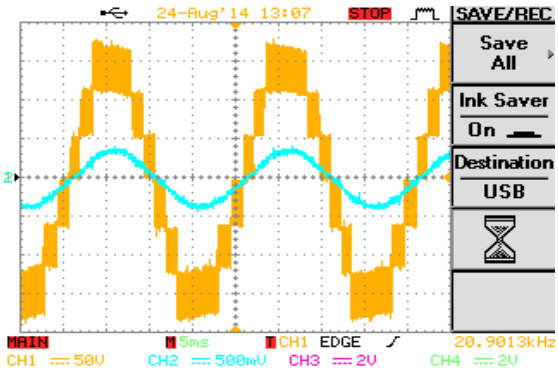

Fig (24). Output voltage and current waveforms of the inverter under asymmetric operating conditions

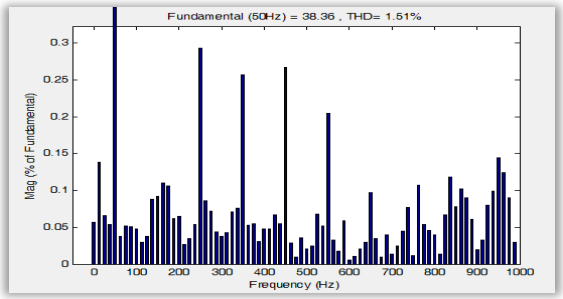

Fig (25): Harmonic component of the output current of the inverter under symmetric condition

Figure 25 shows the harmonic component of the output current of the inverter under symmetric operating condition. According to this figure, the THD of the output current is 1.51%. Although this THD is higher than the value obtained in simulation results, but it still meets ISIRI 11859 standards for current THD, which suggests that a THD less than 5% is acceptable. The difference between simulation results and implementation results has various reasons, where the most important ones are: different periods of different sections of the control system in practice and simulation (due to constraints in practical implementation).

VII. Conclusion

Since the multi-level inverters are useful voltage sources, different models are proposed for reducing the number of switches by improving performance and efficiency. In this paper, a sinusoidal pulse width modulation (SPWM) cascade full-bridge single-phase 7-level inverter with phase shift modulation is designed using a suitable voltage control of low capacitance for asymmetric condition. The obtained results prove the validity of the proposed strategy with high performance under different operating conditions. The simulations were performed in MATLAB environment. Also, for further investigations, a laboratory sample of this inverter was constructed to show the practical effects of the proposed approach.

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