Int. J. Nonlinear Anal. Appl.
Volume 12, Special Issue, Winter and Spring 2021, 1497-1509
ISSN: 2008-6822 (electronic)
http://dx.doi.org/10.22075/ijnaa.2021.5797

Design and implementation of folded QRS detector for implantable cardiac pacemaker

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(Communicated by Madjid Eshaghi Gordji)

Abstract

This paper proposes an area and power efficient technique for the design of an ECG detector. In biomedical applications, like the ECG detector for implantable cardiac pacemaker systems, area and power consumption plays a major role. Thus in this paper, an area-efficient ECG detector with folded pipelined FIR filter is proposed. In conventional wavelet filter bank structure, the decimated wavelet filter bank used makes use of 3 LPFs and 1 HPF of pipelined architecture. This pipelined filter structure requires more hardware. Thus in the proposed architecture folding transformation technique has been applied to the pipelined filter structure in order to reduce the hardware. The decimated wavelet filter bank consisting of the filter structures followed by down samplers is used to denoise the ECG signal. The QRS complex detector consisting of a comparator, counter and a threshold block is used to find the correct location of the QRS complex. In order to further reduce the number of registers that occurs as a result of the folding transformation, folding transformation with register minimization technique is applied to the pipelined filter that results in less hardware utilization. The proposed technique is implemented using Xilinx System Generator. Thus a total area of 22.78 is saved using the proposed method. Considerably a low power of 115mW is also achieved which makes it useful for high-performance medical applications.

Keywords: Implantable cardiac pacemaker (ICP), Wavelet filter bank (WFB), ElectroCardiogram (ECG), Detection error rate (DER)

1. Introduction

For the ageing population, improved health care and cost reduction has become a big challenge. The need for health-care applications, such as implantable medical devices, is fast rising these days.

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Received: August 2021 *Accepted:* November 2021

The cardiac pacemaker, which is implanted in the human body to detect and monitor a person's heart beating rate, is one of the most regularly used biomedical devices. After obtaining aberrant signals from the pacemaker, the appropriate cure is given to the patient. [1]. The cardiac pacemaker's Electrocardiogram (ECG) detector uses digital signals to assess the heart's beating rate and rhythm. The P wave, which depolarizes the atria, the QRS complex, which depolarizes the ventricles, and the T wave, which repolarizes the ventricles, are the three primary components of the ECG. The QRS complex has a bigger amplitude than the P and T waves over the R–R interval of all three waves. The precise detection of R wave is essential in order to monitor the heart beating rate of patients. QRS detection is the cornerstone for practically all ECG analytical methods, as the heart rate and other parameters can be evaluated after the QRS diagnosis to prevent severe diseases. The pacemaker is supposed to work once it is put in the body. with high detection reliability over several years. Low power and area consumption is another critical design criterion to minimise recurrent surgeries due to battery fatigue [6]. A novel way for implementing the ECG detector is proposed in this paper.

The following is how the paper is structured: The first section of the paper is an introduction. The results of the literature review are presented in Section 2. The traditional detector design technique is discussed in Section 3. Section 4 describes the proposed ECG detector design technique. The proposed technique's performance evaluation and simulation results are given in Section 5. Finally, Section **??** brings the paper to a close.

2. Literature review

[1] offers the design of a QRS complex detector using Multi Scaled Product and Soft Threshold algorithms by Bhavtosh and D. Berwal. The QRS complex wave is detected using a radix-4 Booth multiplier. The complexity of this detector is lower. Despite the fact that the overall delay has decreased, the hardware use has increased. Y.J. Min, H.K. Kim, Y.R. Kang, G.S. Kim, J. Park, and S.W. Kim present a wavelet-based ECG detector with wavelet filter banks, a noise detector, and a QRS complex detector for hypothesis testing with wavelet demodulated ECG data in [6]. The detector's detection accuracy is excellent and its power consumption is low, but the hardware utilisation is higher since the wavelet filter bank (WFB) employs a larger number of LPFs and HPFs. The 0.13-um low-leakage UMC technology is used to create the wavelet-based R-wave detector presented [4]. When the patient is not exposed to noise, a mode that shutters roughly two-thirds of the hardware saves power. By including sleep transistors into the power supply's rails, this approach offers the advantage of lowering leakage power. Although the detector's leakage power is lowered, the addition of a noise detector increases the hardware utilisation. The dyadic wavelet transform (DyWT) is used in the construction of the QRS complex detector suggested [8], which is generally robust to time-varying QRS complex based morphology. The suggested DyWT-based detector performs better for ventricular contractions in the early stages, such as couplets tapes and bigeminy. The detector is noise-resistant and offers a lot of versatility when it comes to interpreting ECG data with time-varying features. [9] A method for designing a QRS complex detector is proposed, in which the complexes are identified using a relatively simple morphological operator. In the peak valley, the operator serves as an extractor before being controlled by a structural component. This contributes to an extremely short execution time. One disadvantage of this method is that it requires 24-hour Holter ECG records to fully assess the detector's effectiveness, which is time demanding.

3. Conventional ECG detector

The ECG detector usually consists of two main components : the wavelet filter bank and the QRS complex detector [5].

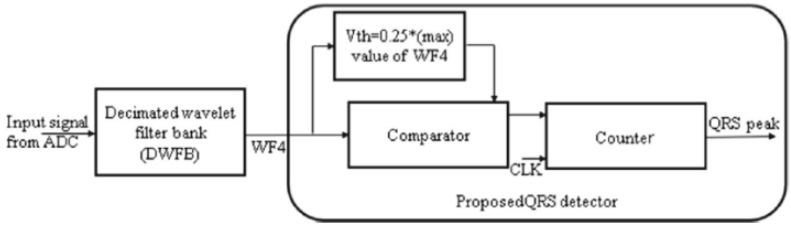

Figure 1: Block Diagram of the ECG Detector

A. Wavelet filter bank

The wavelet filter bank circuit is based on the decimated wavelet transform. There are several wavelet transforms used in general like Dyatic, Haar, Symlet and Biorthogonal wavelet transform [8]. Here biorthogonal 2.2 wavelet transform is used since it has better SNR and resembles an ECG wave. The wavelet filter bank consists of 3 low pass and a high Pass filters namely WFB1, WFB2, WFB3 and WFB4 followed by down samplers [5]. The filter structures are pipelined-based architectures. Pipelining is an important technique used in several applications such as digital signal processing (DSP) systems. It results in the increasing the speed of the critical path The pipelined structure is obtained by introducing delays done by means of cut set introduction to a normal 3-tap FIR filter. The Wavelet Filter banks are used to filter the noise where at each stage the clock frequency gets divided by 2 and finally the original signal is obtained [5]. The Fig.2 shows the wavelet filter bank structure and Fig.3 shows the pipelined architecture of the filter.

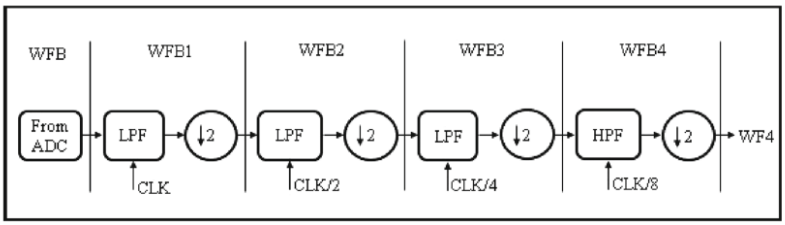

Figure 2: Block diagram of the wavelet filter bank

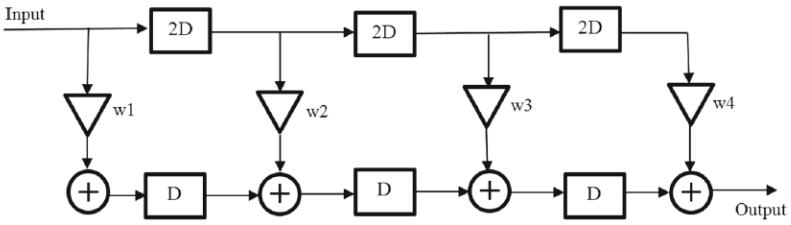

Figure 3: Pipelined architecture of the FIR filter

B. QRS complex Detector

There are two types of thresholds in the QRS complex detector: hard threshold and soft threshold [6]. As illustrated in Fig. 1, the QRS complex detector utilised here comprises of a soft threshold, a comparator, and a counter. The comparator receives the WFB4 output, and the soft threshold (Vth) is set to the maximum value of one fourth of the wavelet filter bank (WFB) output, or 0.25. The wavelet filter bank (WFB) output is compared to the threshold value by the comparator. The output of WFB4 is counted as a peak if it is greater than the threshold; otherwise, it is not counted as a peak. The counter [5] counts how many peaks there are in total.Proposed ECG Detector.

A. Folding

Folding is a technique in which a single functional unit is used which performs many algorithm operations based on time multiplexing. Folding technique thus helps to reduce the number of computational blocks used. Though folding reduces the area occupied in the chip it also leads to increase in the number of registers used in the design. In order minimise the number of registers, register minimization technique is adopted in which the number of register are reduced by means of a life time chart [3, 7].

B. Folding of Pipelined FIR Filter

Let us consider the pipelined FIR filter shown in Fig.3 The filter has folding order N=4 and folding sets $S1 = \{3, 1, 2, 0\}$for adders and $S2 = \{0, 2, 3, 1\}$ for multipliers. The folding equation is given by,

$$D_F(U \rightarrow V) = NW(e) - P_U + v - u \tag{1}$$

Where $W(e)$ represents the weight of the edge, PU represents the pipelined stages, v and u represents the folding order of V and U node respectively [7].

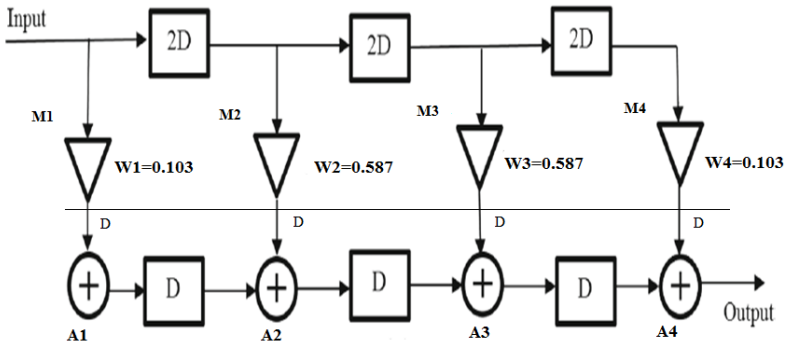

Figure 4: Pipelined FIR filter showing cut set retiming

The folding equation is applied to all the edges present in the filter to find the number of delays present in the folded structure.

$$
\begin{aligned}
&D_F(A1 \rightarrow A2) = 4(1) - 1 + 1 - 3 = +1\\
&D_F(A2 \rightarrow A3) = 4(1) - 1 + 2 - 1 = +4\\
&D_F(A3 \rightarrow A4) = 4(1) - 1 + 0 - 2 = +1\\
&D_F(M1 \rightarrow A1) = 4(0) - 2 + 3 - 0 = +1\\
&D_F(M2 \rightarrow A2) = 4(0) - 2 + 1 - 2 = -3\\
&D_F(M3 \rightarrow A3) = 4(0) - 2 + 2 - 3 = -3\\
&D_F(M4 \rightarrow A4) = 4(0) - 2 + 0 - 1 = -3
\end{aligned} \tag{2}
$$

Since the folding equations consist of negative values for edge $M1 \rightarrow A2, M3 \rightarrow A3, M4 \rightarrow A4$ and it cannot be realized, cutsets are applied in these paths as shown in Fig.4 to perform retiming. The retimed pipelined FIR filter is shown in Fig .4. Again the folding equations are applied to the retimed filter to construct the folded filter.

$$
\begin{aligned}
&D_F(A1 \rightarrow A2) = 4(1) - 1 + 1 - 3 = 1\\
&D_F(A1 \rightarrow A3) = 4(1) - 1 + 2 - 1 = 4\\
&D_F(A3 \rightarrow A4) = 4(1) - 1 + 0 - 2 = 1\\
&D_F(M1 \rightarrow A1) = 4(1) - 2 + 3 - 0 = 5\\
&D_F(M2 \rightarrow A1) = 4(1) - 2 + 3 - 0 = 1\\
&D_F(M3 \rightarrow A3) = 4(1) - 2 + 2 - 3 = 1\\
&D_F(M4 \rightarrow A4) = 4(1) - 2 + 0 - 1 = 1
\end{aligned} \tag{3}
$$

As there are no negative values in the folding equations (14) to (16), the folded architecture can be constructed from the folding sets and the folding equations.

C. Register minimisation technique

In order minimise the number of registers, register minimization technique is adopted in which the number of register are reduced by constructing the life time table [3]. The life time of a node is given by,

$$
\begin{aligned}
&T_{input} \rightarrow T_{output}\\
&U + P_U \rightarrow U + P_U + max_V\{D_F(U \rightarrow V)\}
\end{aligned} \tag{4}
$$

Where T_{input} and T_{output} represents the time instance of input and output variables.

From the life time values shown in table 1. life chart for the retimed FIR filter is constructed as shown in Fig .5.

From Fig.5 it is clear that the maximum number of registers required is 4. By using only 4 registers data allocation table is constructed as shown Table 2.

Using the data allocation table as shown in the above table, the folded pipelined filter with minimum number of registers is shown in Fig.6.

4. Simlulation results and discussions

A. Filter design using FDA tool

The Filter Design and Analysis Tool is used to create the FIR filter (FDA Tool). The standard ECG ranges from 0.05 to 100 Hz, however higher frequencies can also be found in the signal [4]. For

Table 1: Lifetime for retimed pipelined FIR filter

Nodes	Tinput	→Toutput
A1	4	4 → 5
A2	2	2 → 6
A3	3	3 → 4
A4	4	1 → 1
M1	5	2 → 7
M2	6	4 → 5
M3	7	5 → 6
M4	8	3 → 4

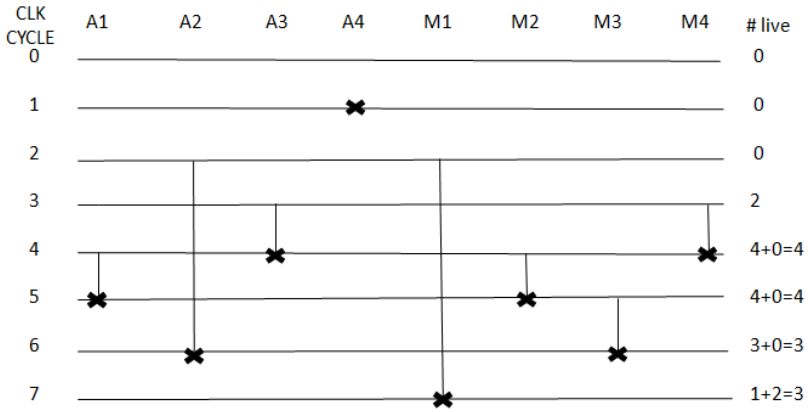

Figure 5: Life time chart for the retimed FIR filter

Table 2: Folded pipelined FIR filter

Clock	Input	R1	R2	R3	R4	Output
0						
1	A4					A4
2	A2,M1					
3	A3,M4	A2	M1			
4	A1,M2	A3	A2	M1	M4	M4,A3
5	M3	A1	M2	A2	M1	A1,M2
6		M3		M1	A2	M3,A2
7				M1		M1

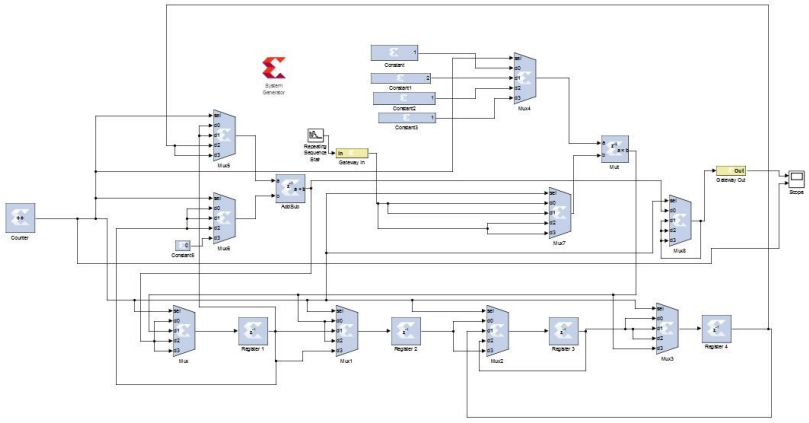

Figure 6: Folded pipelined FIR filter

the high frequencies signal to be retained, the incoming ECG signals must be sampled (digitised) at least twice the rate of the highest frequency of interest. Otherwise, the signals will be corrupted. This means that the sample rate must be at least 500 Hz if the frequency range of interest is 150-250 Hz. In actuality, a larger sampling rate is required, hence sampling rates of 1000 Hz or higher have been used in most high frequency applications.

The FDA tool is used to determine the filter properties, and the filter coefficients are acquired for both pipelined Low pass and High pass filters. The order of the filters is 3. The Fig.7 shows the setting of FDA tool.

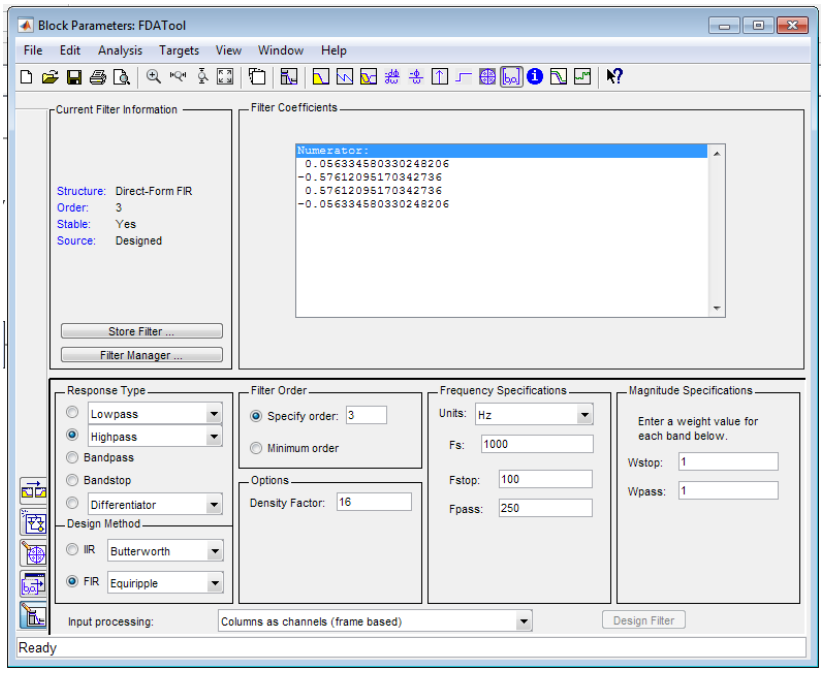

Figure 7: FDA tool design wizard

B. Wavelet filter bank implementation using system generator

The decimated wavelet filter bank is implemented in system generator as shown in Fig.11 using the above specification. The filter coefficients are taken from the FDA tool. The filter bank consists

of pipelined LPFs and HPFs as shown in Fig.8 The filter is tested using the .mat files taken from MIT-BIH arrhythmia database. The noise signals are added to the ECG signal and finally the filtered output is obtained. The output of the wavelet filter bank for a input of 100.mat ECG signal is shown in Fig.10.

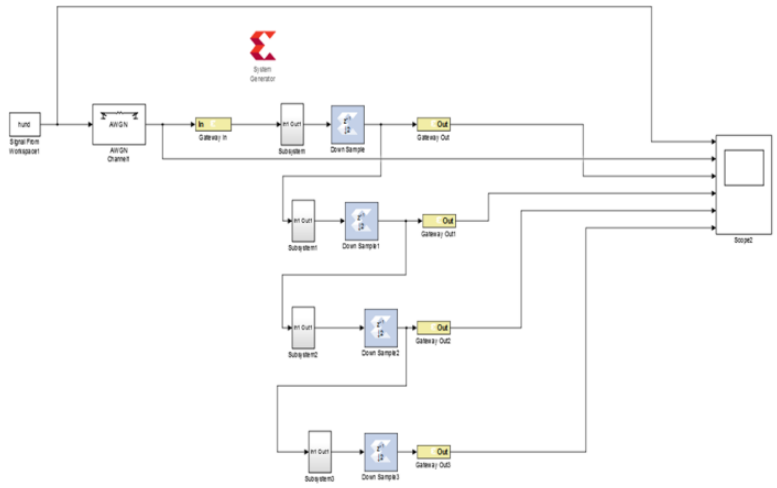

Figure 8: Decimated wavelet filter bank

The subsytem of the filter bank which is the pipelined FIR filter structure is shown in Fig.9.

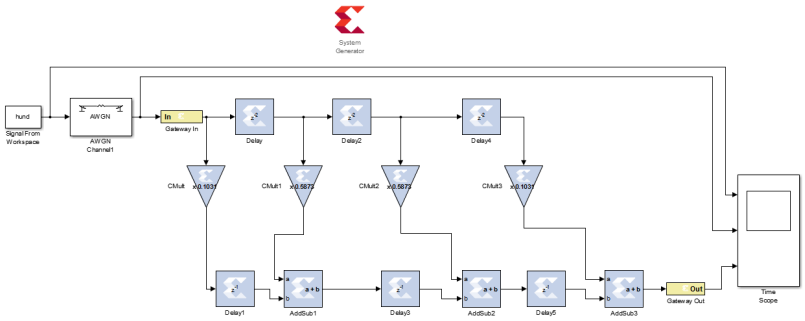

Figure 9: Pipelined FIR filter implementation

The output waveforms for nearly 10 samples of ECG signal taken from the MIT-BIH Arrhythmia database were obtained. The output waveform for .100 mat file is shown in Fig.10.The first window in Fig.10 shows the input ECG signal, the second window shows the noise added input signal,window three, four and five shows the output of LPF's after each stage of noise filteration.The window six shows the output of HPF which is the final reconstruted input signal after noise removal.

C. Implementation of QRS complex detector

The QRS complex detector circuit is design with a soft threshold block, a comparator and a counter. Output of the WF4 is given to the comparator and a soft threshold is set at the maximum value of one fourth that is 0.25 of the wavelet filter bank output. The comparator compares the wavelet filter bank (WFB) output with the threshold value. If the output of WFB4 is greater than

the threshold, it is counted as a peak otherwise no peak is counted. The total number of peaks is counted by the counter.

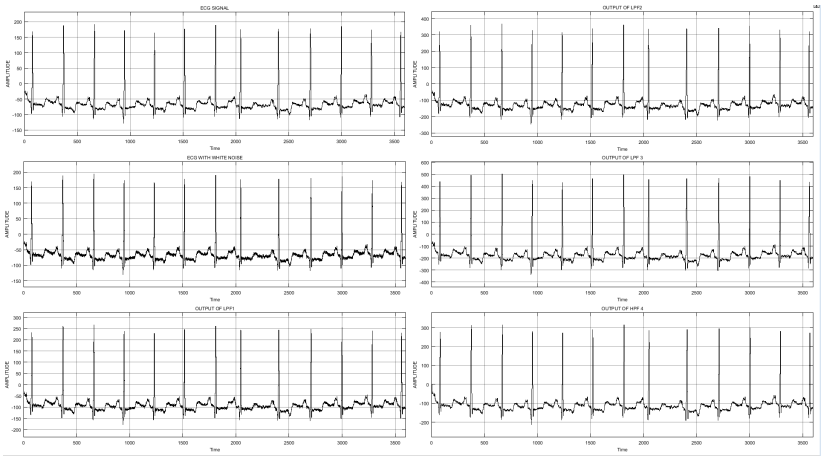

Figure 10: Output of Decimated Wavelet Bank for an input of 100.mat ECG signal

The output waveforms for nearly 10 samples of ECG signal taken from were taken. The output waveform for .100 mat file is shown in Fig.12 the first window shows the input ECG sisgnal,second window shows the noise added input signal and the last one shows the detection of a QRS Complex.

The implementation of the QRS complex detector for an input of 100.mat ECG signal is shown in Fig.11.

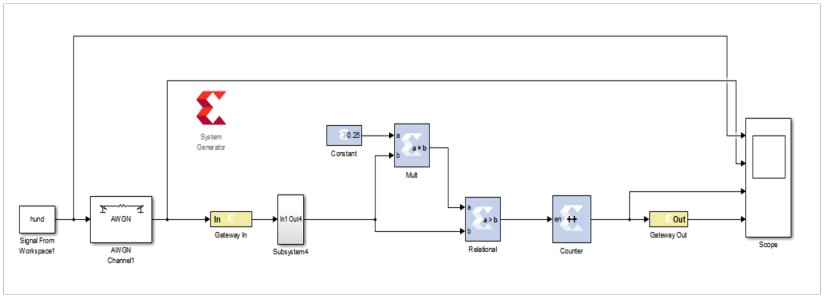

Figure 11: Implementation of QRS complex detector

D. Performance parameters

The performance parameters for the ECG detector such as sensitivity (Se), predictivity ($P+$) and Detection Error Rate (DER) for different samples of ECG signal are calculated and tabulated [2].

Sensitivity (Se) is given as follows

$$Se = \frac{TP}{TP + FN}\% \tag{5}$$

Where TP is the true positive which represents the number of correctly detected QRS complexes and FN is the false negative which denotes the number of missed detections.

Positive predictivity ($P+$) is given as follows

$$P^{+} = \frac{TP}{TP + FP}\% \tag{6}$$

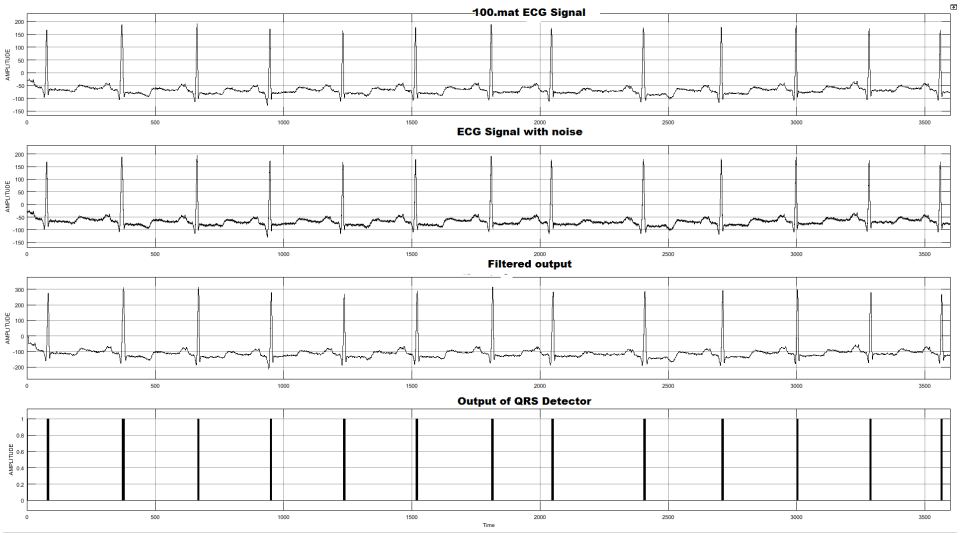

Figure 12: Output of QRS complex detector for an input of 101.mat ECG signal

Where FP is the false positive which denotes the detection of false QRS complexes.

Detection Error Rate (DER) is calculated using

$$DER = \frac{FP + FN}{TOTAL\ NUMBER\ OF\ QRS\ COMPLEXES}\% \tag{7}$$

Table 3: Performance parameter of the pipelined filter based ECG detector for different samples of ECG signal using 10 second MIT-BIH database

ECG Signal	**Total (beats)**	**TP (beats)**	**FN (beats)**	**FP (beats)**	**Se (%)**	**P^+ (%)**	**DER (%)**
100	13	0	0	0	100	100	0
101	13	13	0	1	100	92.85	0.07
102	12	11	1	0	91.66	100	0.08
103	14	13	1	1	92.85	92.85	0.14
104	13	13	0	0	100	100	0
105	11	11	0	1	100	92.85	0.07
106	13	12	1	0	92.30	100	0.07
107	12	11	1	0	91.66	100	0.08
108	11	11	0	0	100	100	0
109	14	14	0	1	100	92.85	0.06
Total	126	122	5	5	96.84	97.14	0.07

Thus a sensitivity of 96.84%, positive predicitivity of 97.14% and Detection Error Rate (DER) of 0.07% is achieved using the pipelined filter based ECG detector circuit for 10 second MIT-BIH Database.

Table 4: PERFORMANCE PARAMETER OF THE PIPELINED FILTER BASED ECG DETECTOR FOR DIFFERENT SAMPLES OF ECG SIGNAL USING 1 minute mit-bih database

ECG Signal	**Total (beats)**	**TP (beats)**	**FN (beats)**	**FP (beats)**	**Se (%)**	**P^+ (%)**	**DER (%)**
100	75	75	0	0	100	100	0
101	74	73	1	0	98.64	100	0.013
102	74	74	0	0	100	100	0
103	71	71	0	1	100	98.61	0.014
104	74	74	1	0	98.66	100	0.013
105	70	70	0	1	100	98.59	0.014
106	73	72	1	0	98.63	100	0.013
107	79	76	2	0	97.43	100	0.025
108	70	70	0	2	100	97.22	0.028
109	75	75	0	0	100	100	0
Total	735	730	5	4	99.33	99.44	0.12

E. Resource utilization of ECG detector

The system created in system generator is converted to HDL netlist. For synthesis Zedboard and Zynq Evaluation board is selected and imported to Xilinx Vivado 2016.2 and then the analysis of resource utilization, power and delay consumption is done. The overall resource utilization of the pipelined filter and folded filter structures and the total area saved is as shown in Table 5.

Table 5: Comparison of resource utilization of the existing and propopsed architectures

IMPLEMENTATION	**Slice LUTs (Out of 53200)**	**Slice Flip Flops (Out of 106400)**	**Slice DSPs (Out of 220)**	**Slice IOs (Out of 200)**	**Slice LUT RAMs (Out of 17400)**	**Overall percent of resource used (%)**
Conventional Pipelined FIR Filter	188	147	0	33	48	22.12
Proposed Folded Filter	104	105	1	33	48	17.08
Total Area Saved in (%)						22.78

The power consumed by the sytem using pipelined filter structure is shown in Fig 13.

The power consumed by the system using folded filter structure is shown in Fig.14.

Thus it can be seen that a total area of 22.78% is saved using the proposed technique. The total on chip power of the proposed circuit using folded filter structure is only 0.115W.

F. Comparison of proposed architecture with existing method

The comparison of total hardwares used between the proposed method and the existing method is shown in Table 6.

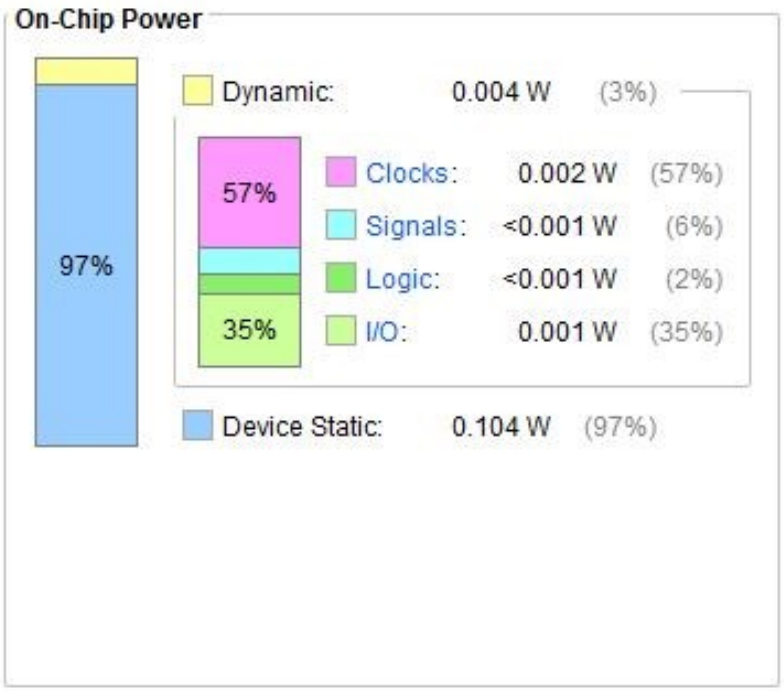

Figure 13: Power consumed by the system using pipelined filter structure

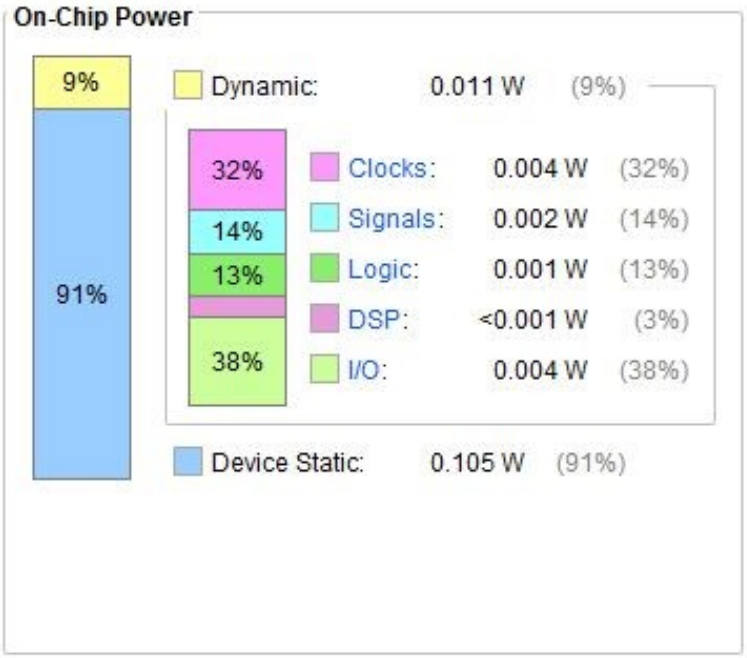

Figure 14: Power consumed by the system using Folded filter structure

Table 6: Comparison of hardwares between proposed Architecture and existing method

Hardwares used	**Conventional ECG detector (Pipelined FIR filter based)**	**Modified ECG detector (folded FIR filter based)**
Adder	4	1
Multiplier	4	1
Registers	9	4

5. Conclsion

An area efficient ECG detector for Implantable Cardiac Pacemaker Systems is proposed in this paper. The hardware efficient wavelet filter bank consisting of low pass and high pass filter structures help in the filtering of noise added ECG signals. The R-wave peak detection is also achieved by means of the QRS complex detector. Thus reduced hardware utilization is achieved by applying folding transformation with register minimization technique to the pipelined FIR filter. A total area of 22.78% is saved using the proposed technique. The total on-chip power consumed by the detector is also considerably less which is 115mW. This makes the design hardware and power efficient. The proposed methodology can further be extended to areas of data compression of ECG signals using Run-Length Encoding (RLE) technique.

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