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FIR and folded IIR filter designs for speech processing in hearing AID

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Abstract

Abstract—The present trend of low power and area has led to the design of many efficient algorithms for speech processing in portable devices. In biomedical applications like hearing aid, high performance is not the key area of interest. Area and power also play a major role. There are many factors which affect the market penetration. So, the system can run as slow as possible to trade speed for power and area. An area efficient folded IIR filter is designed. The folded architecture uses the concept of time multiplexing and it has only one multiplier and one adder to perform all the operations. Thus, the area is reduced, and this filter is converted into an IP. The area and resource utilization of the folded IIR filter is compared with the normal IIR filter design. AFIR filter is also designed and converted into an IP.This FIR IP is used in the block design to process a corrupted audio signal. Zed board is a part of Xilinx zynq -7000 All Programmable SoC. It consists of processing system and programming logic. The filter design is implemented in the programming logic part. The design is synthesized and the bitstream in generated. The generated bitstream along with the hardware is exported to SDK where the corrupted audio signal is processed on zed board.

Keywords: Low power, IP, multiplexing, SoC, Processing system, Programming logic

1. Introduction

Today around 17% of the population in the world are suffering with hearing loss. In a noisy environment, the speech intelligibility further deteriorates. A hearing-impaired person requires a

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hearing aid that is adaptable and flexible with the external environment, improved signal to noise ratio and increased speech intelligibility in noise. A hearing aid is nothing but a small electronic instrument that amplifies the sound so that a hearing-impaired person can listen and communicate.

Low power and area has always been the keen factors in the market. This led to the design of many efficient algorithms for speech processing in portable devices. In biomedical applications like hearing aid, high performance is not the key area of interest. Area and power also play a major role. There are many factors which affect the market penetration. One such factor is the lack of versatility. The devices amplify all types of sounds including noise.

A hearing aid is preferable in market if it has the following features

- Small size
- Long life time
- Good speech intelligibility
- Adaptable to the environment
- Low latency

There is always a trade of between power, area and latency. If we want a portable, area efficient device then we must compromise on power and latency. Similarly, if we want a highspeed device then we must compromise on area and power. So, there is always a trade of among the devices. Many algorithms and architectures are proposed which are area efficient and low power devices. In this paper, area is considered as the key parameter and hence an efficient folded architecture is used to implement the filter in a hearing aid.

2. Folded in finite impulse response response filter

A. IIR Filter

IIR filters are also called as recursive filters because of their recursive structure which is nothing but the feedback path from output to input. They contain both feedforward and feedback path. IIR filters can be implemented in different structures. The basic equation of an IIR filter is given as [7].

$$y[n] = \sum_{l=1}^{N} a_l y[n-1] + \sum_{k=0}^{M} b_k x[n-k] \tag{1}$$

where a_l and b_k are filter coefficients, $x[n]$ and $y[n]$ are input and output sample values, M and N are the order of the filter.

The general structure of Nth order IIR filter is as shown in Fig 1.For an Nth order IIR filter we require 2N delay elements, $2N+1$ multiplier and $2N$ adders to implement the filter.

Consider a second order IIR filter as shown in Fig 2. It requires 4 delay elements, 5 multipliers and 4 adders. It is implemented in direct form-1 structure.

If efficient area utilization is our primary goal, then direct form -2 structure is preferred. Its structure is shown in Fig3. It has reduced delay elements when compared with direct form1 structure [7].

A second order IIR filter with two poles and two zeros is called as a digital biquad filter. To further reduce the area, folding transformation is applied to the retimes biquad filter.

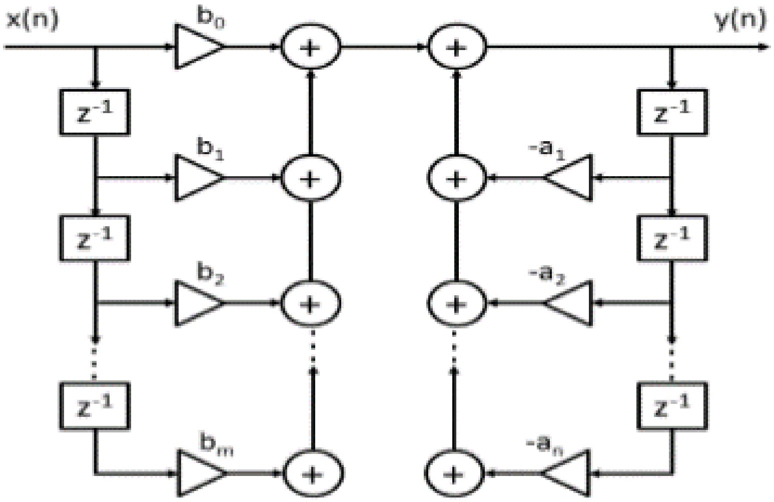

Figure 1: Nth Order IIR filter structure

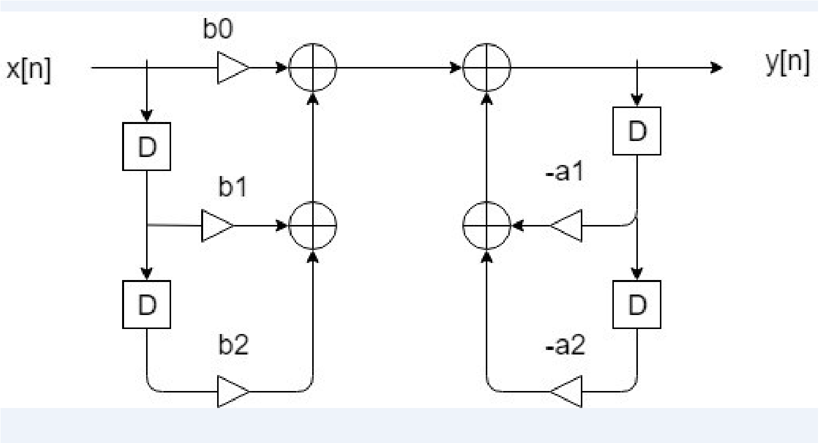

Figure 2: Direct form -1 IIR filter

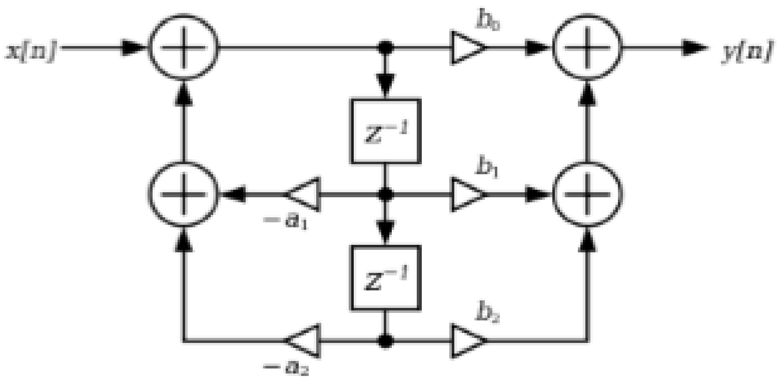

Figure 3: Direct form – II IIR filter design

B. Folding

Folding transformation is a technique in which single functional unit is used to perform all the operations of the algorithm using the concept of time multiplexing [8]. Consider the following example in which we must perform the addition of three numbers namely $a[n], b[n], c[n]$. We need two adders to perform this task. The first adder is used to perform the addition of $a[n]$ and $b[n]$. The result obtained from the first adder is given as input to the second adder along with $c[n]$. The final result is obtained as the output of the second adder and it is given as $y[n]$. The structure is shown in Fig 4.

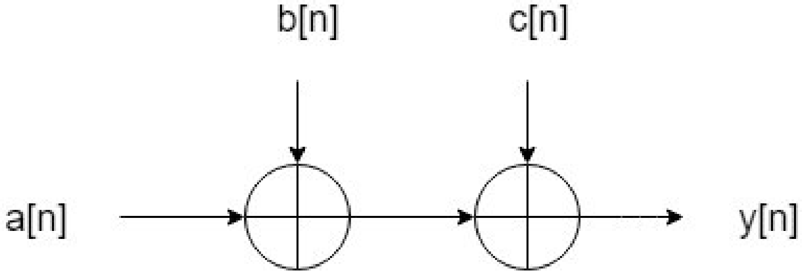

Figure 4: Adder

The task of addition of three numbers can be performed on a single adder using the concept of folding as shown in the Fig 5. By doing so we can reduce the hardware required and hence the circuit becomes area efficient. In the first clock cycle the addition of $a[n]$ and $b[n]$ is performed. The output from the adder is stored in a register and is fed back again as input to the adder in the next clock cycle. This partial product from the register is added along with $c[n]$ in the next clock cycle. The folding factor is two ($N = 2$) because we get the output after two clock cycles and the input must be fed after every two clock cycles. Folding Factor is defined as the number of operations that are to be performed on a single functional unit. During the two clock cycles the input must be stable and it must not change.

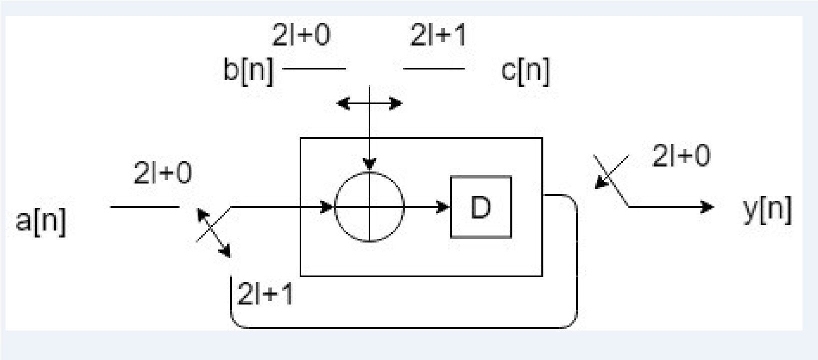

Figure 5: Folded adder structure

C. Folding of a biquad filter

For area efficient circuit, folding transformation is applied to the retimed biquad filter which is shown in Fig 6. Retiming is a technique applied to the circuit to reduce its clock period, power consumption and sometimes even logic synthesis. It is a process of changing the position of delay elements in the circuit in such a way that its input and output characteristics remain same. Its functionality must remain unaltered.

It is assumed that adder requires 1ut and multiplier requires 2ut. Mathematically it is given by$Pa = 1$, $Pm = 2$. The retimed biquad filter is folded with a folding factor of 4 which means that each node in the given figure is executed after every 4 clock cycles. The folded biquad filter

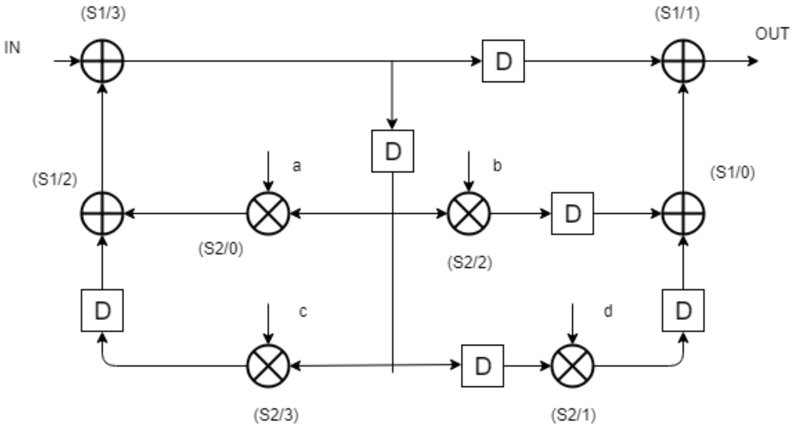

Figure 6: Biquad filter

architecture is shown in Fig 7. The folding sets are given by $s_1 = \{4, 2, 3, 1\}$ and $s_2 = \{5, 8, 6, 7\}$ [4, 6, 5]. S1 represents the time instant at which the corresponding addition operation is performed. During the first time instant $(4l + 0)$, 4th adder operation is performed on the given functional unit. During the second time instant $(4l + 1)$, 2nd adder operation is performed. During the second time instant $(4l + 2)$, 3rd adder operation is performed. During the fourth time instant $(4l + 3)$, 1st adder operation is performed. In this way, four addition operations are time multiplexed and are performed on a single functional unit.

Similarly, multiplication operation is also time multiplexed and is performed on a single functional unit. During the first time instant $(4l + 0)$, 5th multiplier operation is performed on the given functional unit. During the second time instant $(4l + 1)$, 8th multiplier operation is performed. During the second time instant $(4l + 2)$, 6th multiplier operation is performed. During the fourth time instant $(4l + 3)$, 7th multiplier operation is performed.

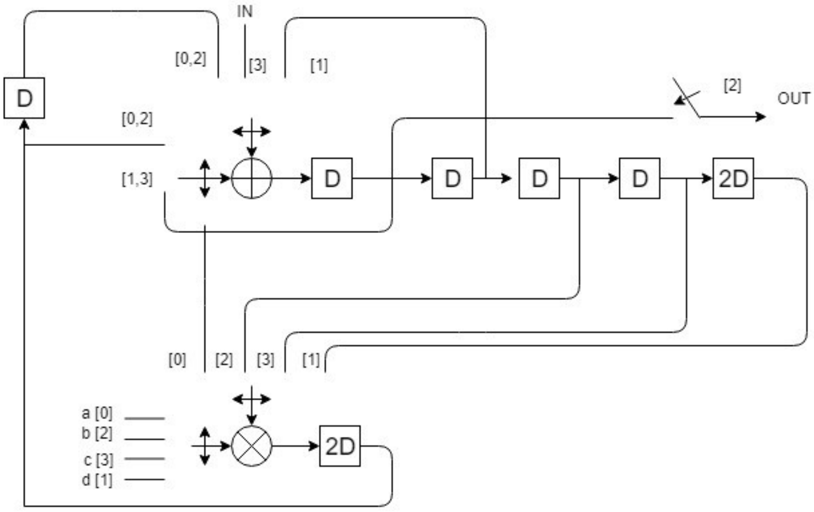

Figure 7: Folded biquad filter

The folded structure of the given biquad filter is obtained by computing the delay elements among each pathusing the formula [8].

$$D_F(U \to V) = Nw(e) - P_u + v - u$$

Where N=Folding factor $w(e)$ = Number of delay elements between the edges u to v.

For the 11 edges present in the filter, the number of delay elements present in the folded data flow graph are computed.

$$\begin{aligned}
D_F(1 \rightarrow 2) &= 4(1) - 1 + 1 - 3 = 1\\
D_F(1 \rightarrow 5) &= 4(1) - 1 + 0 - 3 = 0\\
D_F(1 \rightarrow 6) &= 4(1) - 1 + 2 - 3 = 2\\
D_F(1 \rightarrow 7) &= 4(1) - 1 + 3 - 3 = 3
\end{aligned} \tag{2}$$

$D_F(1 \rightarrow 7) = 3$ represent that we have an edge with three delay elements between the adder to multiplier. In this way the folded structure is constructed and is implemented using Verilog HDL in Vivado. This filter is converted into an IP and it is instantiated in the block design.

3. FIR filter implementation on ZED board

A FIR filter is designed to process a corrupted audio signal. The filter is designed using sequential algorithm. The coefficients are loaded from another DAT file. A dat file consist of data in binary or text format. This filter is converted into an IP and in used is the block design.

The block design is created to target the Zed Board from the "Xilinx Zynq-7000 All Programmable SoC". It consists of two parts namelyPS (Processing System) and PL(Programmable Logic) which constitute an SoC (System on Chip) style [1, 9]. A processing system IP wrapper is created which act as an inter-connection between the processing system and programmable logic. This design is synthesized, and a bit stream is generated.

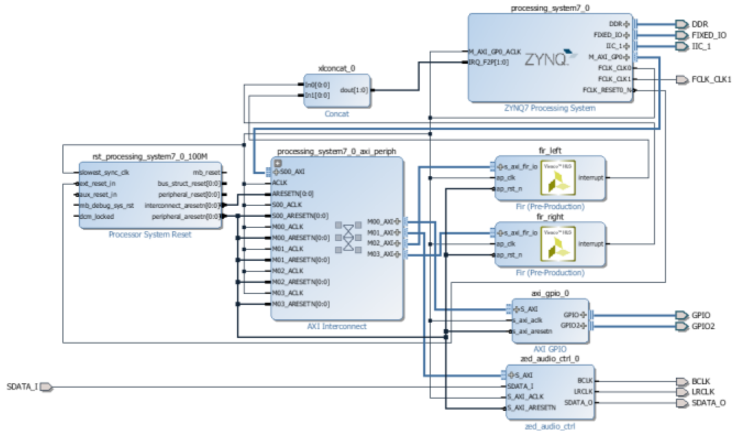

Figure 8: Block design using FIR filter

The generated bit stream is exported to the hardware which means an hdf file is created and it is exported to the SDK. The hdf (Hierarchical Data Format) file format is used to handle large size data[2, 3]. This data contains the block design bitstream and other required information.

A test application is created and run on the board. The FPGA is programmed, and the corrupted audio signal is given to the FPGA using an audio jack. The output is taken from the output port on the board and it is heard using a speaker.

4. Results

The basic IIR filter and the folded biquad filters are designed using Verilog HDL. These designs are implemented on Vivado platform. The basic IIR filter is implemented in direct form – II structure.

The designs are synthesized, and the hardware used for both the architectures are compared. The schematic of IIR filter design is shown in Fig 9.

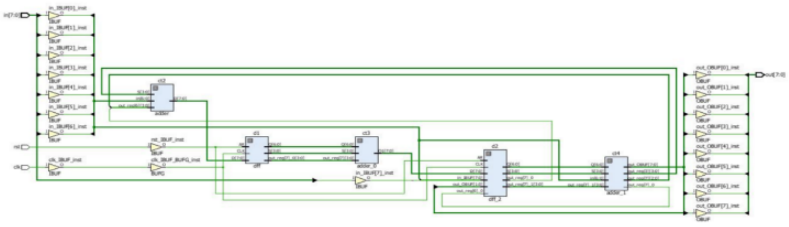

Figure 9: Schematic of IIR filter

Folded biquad filter uses one multiplier and one adder to perform all the operations. The schematic of a folded biquad filter is shown in Fig 10.

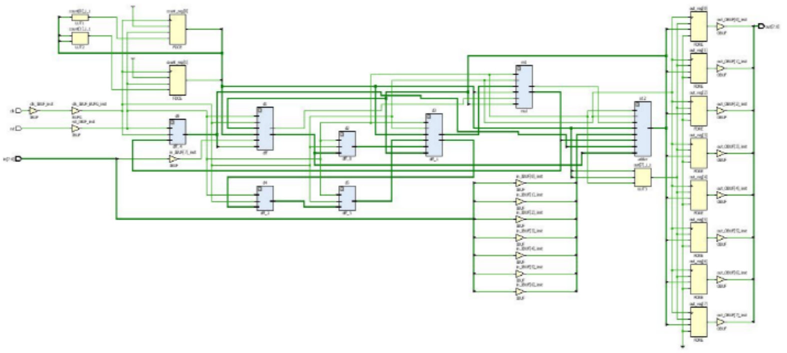

Figure 10: Schematic of folded biquad filter

5. Resource utilization of the filters

The direct form – II IIR filter and the folded biquad filter is implemented in Xilinx Vivado. The area and resource utilization of the two filters are compared.

Table 1: Resource utilization of IIR filter

Resource	Estimation	Available	Utilization
LUT	26	20800	0.13
FF	16	41600	0.04
IO	18	106	16.98
BUFG	1	32	3.13

The direct form – II structure consist of four adders, five multipliers and two delay elements. Its corresponding area and resource utilization are mentioned in Table 1.

The folded biquad filter uses the concept of retiming and multiplexing to perform all the arithmetic operations using one multiplier and one adder. The resource utilization of folded biquad filter is tabulated in the Table 2. The LUT utilization is reduced from 0.13 to 0.09 because of the concept of folding. The flipflop count has increased because in the folded architecture more registers are used when compared with a normal structure. The IO and BUFG utilization remains the same.

Table 2: Resource utilization of folded biquad filter

Resource	Estimation	Available	Utilization
LUT	18	20800	0.09
FF	54	41600	0.13
IO	18	106	16.98
BUFG	1	32	3.13

6. Conclusion

An area efficient folded IIR filter is designed. Its performance is compared with a normal IIR filter implemented in direct form -2 structure.A FIR filter is implemented in Vivado HLS and it is instantiated in the block design. This design is synthesized and bitstream is generated. This generated bitstream is exported to SDK and it is dumped on the zed board. The corrupted audio signal is processed, and the noise is reduced in the signal.

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