N^+ Pocket Core-Shell Nanotube Tunnel Field-Effect Transistor

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Abstract— **One of the attractive candidates for improving the performance of tunnel transistors is cylindrical structures due to their impressive electrostatic control of the gate. But the on-state current of tunnel transistors is still very low compared to MOSFETs. An alternative is to use core-shell nanotubes rather than nanowires. In this article, we present a core-shell TFET nanotube based on a heterogeneous germanium/silicon structure. In our proposed structure, an N^+ pocket is employed to enhance the on-state current. A possible manufacturing method is also proposed that is fully compatible with CMOS technology. The main parameters of this transistor are 97.85 µA / µm on-state current, I_{on} / I_{off} ratio of 8.26×10^8, SS_{avg} mV/dec 21.15, and f_T of 878.95 GHz.**

***Index Terms*—Tunnel FET, germanium-source, core-shell nanotube, heterojunction, on-state current.**

I. Introduction

In recent years, MOSFET transistors have faced serious design and manufacturing challenges due to their short channel effects [1]. Lack of proper control over the source Fermi tail has restricted the subthreshold slope of these transistors. [2]. Due to the need of the semiconductor industry for a device with less power loss, different devices have been designed and proposed, in recent years [3]- [5]. One of the most important structures that do not pose a new challenge to manufacturing technology is Tunnel transistors due to their physical similarities to MOSFETs. The operating mechanism of these transistors, unlike MOSFETs, is to tunnel the carriers through the potential barrier. Like all semiconductor devices, they face challenges such as ambipolar conductivity and low on-state current [6], [7]. Different structures have been designed and proposed, to overcome these limitations [8] - [12]. Nanotube structures are one of the most interesting ideas to improve the performance of tunnel transistors [13].

In nanotubes, in addition to the shell gate, there is also a core gate which increases the electrostatic integrity of the gate and increases the intensity of the electric field at the tunneling junction. Musalgaonkar et al. presented a misaligned nanotube in which the shell gate overlaps with the source [14]. Apoorva et al. proposed dopingless nanotubes with high on-state current [15]. Hanna et al. Proposed germanium-based nanotubes with the on-state current of 18µA/µm at the V_{GS}=1.0V [16]. In this paper, we present a new core-shell nanotube that uses an n^+ pocket between source and channel. This n+ pocket increases the electric field and hence the band bending. This article consists of the following sections. In section II, we introduce the physics of structure, the manufacturing process, and the simulation method. In Section III, we assess the impact of different parameters on device performance. In section IV, we conclude the obtained results.

II. Device Structure, Fabrication Process, and Simulation Methodology

Fig.1 shows the cross-sectional (top) and cylindrical (bottom) shapes of the CSNT-TFET, respectively. As shown in the figure, our proposed device consists of core and shell gates that overlap the pocket and channel area. To increase the on-state current, germanium is used in the source area, which has better tunneling characteristics than silicon [17]. The work- function of the gate metal is 4.3eV. The contact radius of the core gate contact and the core gate are 5nm and 50nm, respectively. All other design parameters are listed in the Table I.

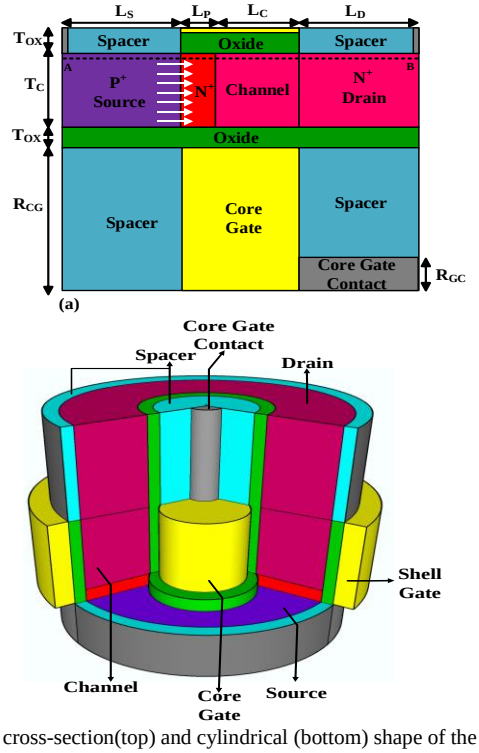

Fig. 1. A cross-section(top) and cylindrical (bottom) shape of the proposed TFET structure (CSNT-TFET).

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TABLE I
Default Values of Proposed TFED Parameters

Dimensions (nm)		Doping concentrations (cm^{-3})	
Epi-layer length, L_P	5	n^+ epi-layer, N_E	4×10^{19}
Source region length, L_S	30	Source region, N_S	2.5×10^{19}
Channel region length, L_C	50	Drain region, N_D	3×10^{18}
Drain region length, L_D	30	Channel region, N_C	1×10^{15}
Channel thickness, T_C,	10		

The operation mechanism of our device is described as follows. As the gate voltage increases, the electrons in the source region tunnel into the channel (Fig. 2 (a)) and then, with the increase of drain current move toward the drain region of the transistor (Fig. 2(b)).

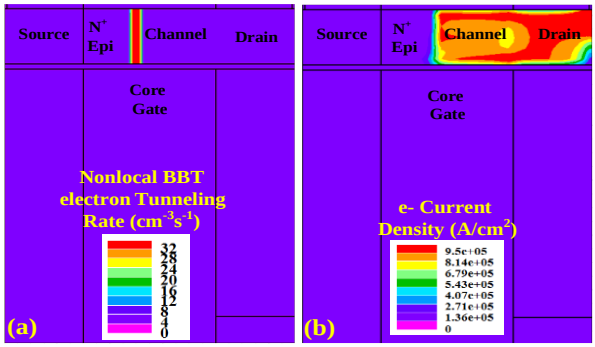

Fig. 2. (a) Electron BTBT tunneling rate, and (b) electron current density contour maps at V_{GS} = 0.5V and V_{DS} = 0.5V.

Fig. (3) indicates the proposed CSNT-TFET manufacturing process. This process begins with the epitaxial growth of germanium in the active silicon region, followed by the growth of n-epi, channel and drain region 3(a). Silicon and germanium layers are selectively etched, then sacrificial oxide and a dielectric layer are deposited 3(b). Gate oxide and gate metal are deposited 3(c). Gate metal is selectively etched, and a layer of SiO_2 and sacrificial oxide are deposited 3(d, e). The sacrificial layer is etched 3(f). A layer of dielectric is removed, the silicon region is etched, and a layer of gate oxide is deposited 3(g). Inner gate metal and a layer of SiO_2 are deposited 3(h), and finally, source, gate, and drain contacts are connected 3(i).

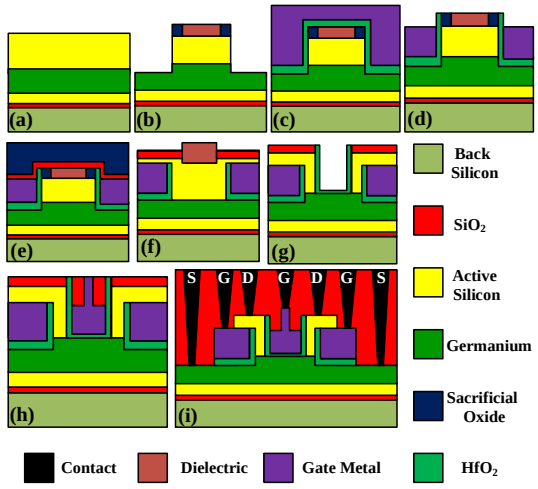

Fig. 3. Fabrication process flow for realizing proposed structure.

All simulations are performed with Silvaco ATLAS [18]. A dynamic non-local band-to-band tunneling model has been used for the proper calculation of the drain current. The generation-recombination of carriers is modeled with the SRH model. The effect of parameters such as doping and temperature on carrier mobility is modeled by CVT. The BGN model is activated due to high doping in the source region. The quantum confinement model is not activated since the length of the pocket region is more than 4 nm [19]. The gate leakage current model is also not activated.

III. Simulation Results and Discussion

Fig.4 indicates the effect of gate voltage on CSNT-TFET energy band diagrams. From the figure, it can be inferred that as the gate voltage increases, the bending of the band increases and we have a larger tunneling window for carriers to tunnel to the conduction band.

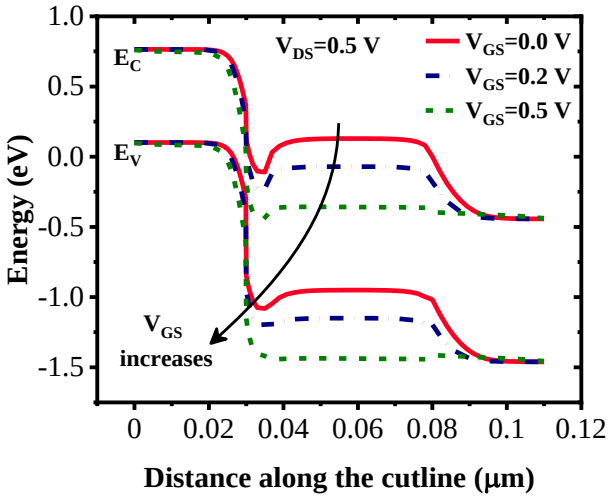

Fig. 4. Impact of gate voltage on the energy band diagram of CSNT-TFET.

In Fig. 5 (a), (b) impact of gate voltage and drain voltage on the drain current of the transistor is assessed. Fig. 5(a) shows that with the increase of gate voltage from V_{GS}=0.1V to V_{GS}=0.5V, drain current increases from 4.46×10^{-3} μA to 33.8 μA, which is mainly due to the reduction of band-to-band tunneling distance. Fig. 5(b) shows that increasing the drain voltage and, hence the increase of the density of states has a low impact on the drain current. It should also be noted that increasing the drain current does not affect the onset voltage of the transistor.

One of the important parameters that have a significant impact on the transfer characteristics of tunneling field-effect transistors is source doping. As shown in Fig.6, with the increase of N_S from 1×10^{19} to 2.5×10^{19}, drain current reaches from 4.02×10^{-1} μA to 33.8 μA which is attributed to the increases of available carriers for tunneling to the conduction band of the channel. Moreover, with the increment of source doping, onset voltage decreases from V_{GS}=0.08V to V_{GS}=0.02V.

One of the main drawbacks of tunneling field-effect transistors is traps in the semiconductor bandgap [20], which dramatically affect the off-state current in heavily doped p-n

junctions. Fig. 7(a) indicates the impact of the TAT model on the transfer characteristics of the CSNT-TFET. In the presence of TAT, the off-state current reaches from 5.9×10^{-12} µA to 4.09×10^{-8} µA. As shown in the inset of Fig (7(a), with the increase of off-state current, the I_{on}/I_{off} ratio decreases from 5.72×10^{12} to 8.26×10^{8}.

Another vital parameter that has a significant effect on the performance of tunneling field-effect transistors is temperature.

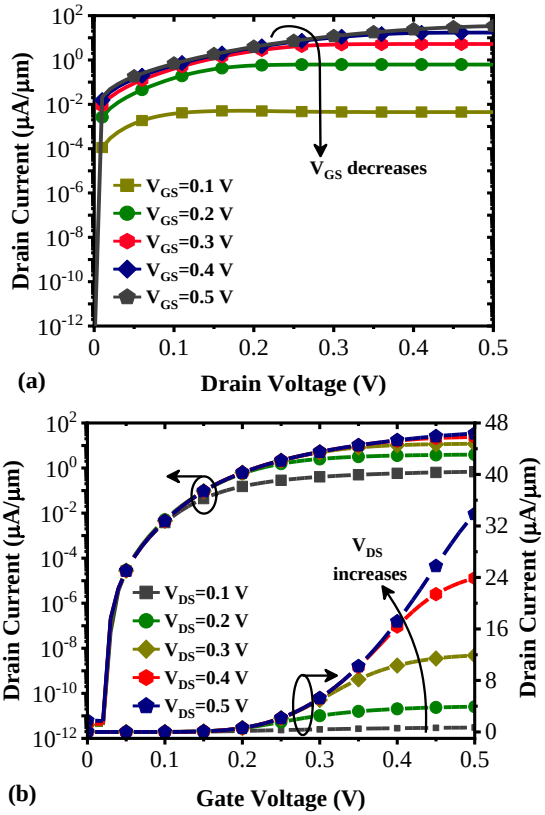

Fig.5. (a) output characteristics for different gate voltages, (b) transfer characteristics for different drain voltages of CSNT-TFET.

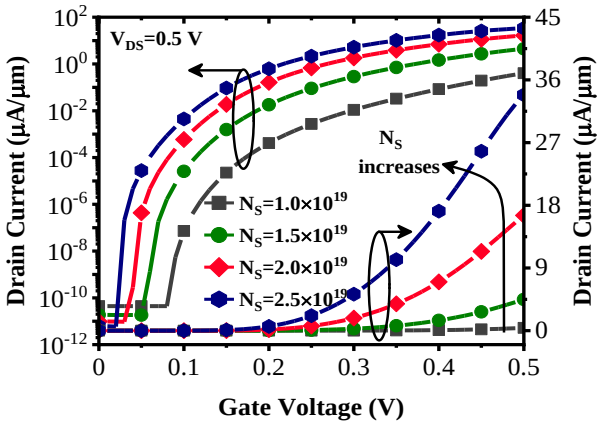

Fig. 6. Impact of N_S doping density on the transfer characteristics of CSNT-TFET.

Fig. 7(b) depicts that, with the increases of the temperature from 300ºK to 375ºK, off-state current with the three decades of current increment reaches 6.11×10-9 µA, which is mainly semiconductors. On the other hand, the on-state current has less sensitivity to the temperature since the tunneling equation has no direct relation to the temperature.

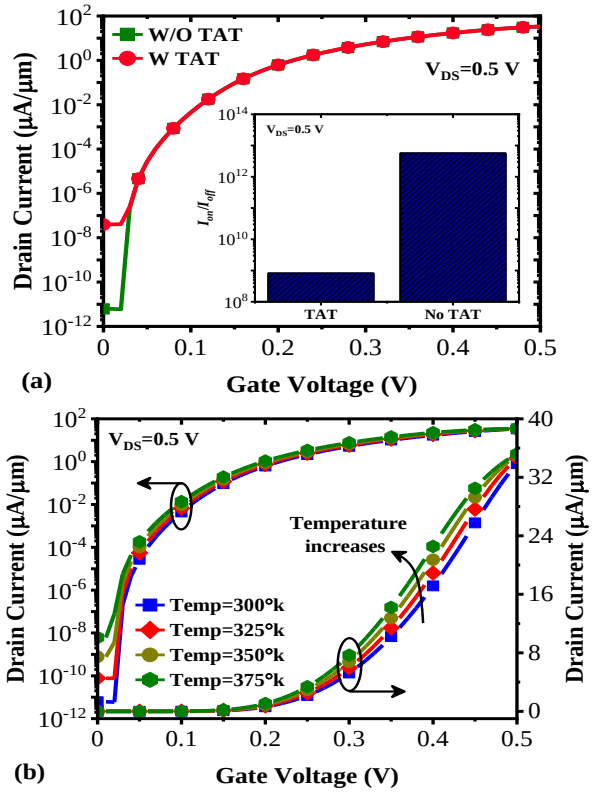

Fig. 7. Impact of TAT (a) and temperature (b) on the transfer characteristics of the CSNT-TFET.

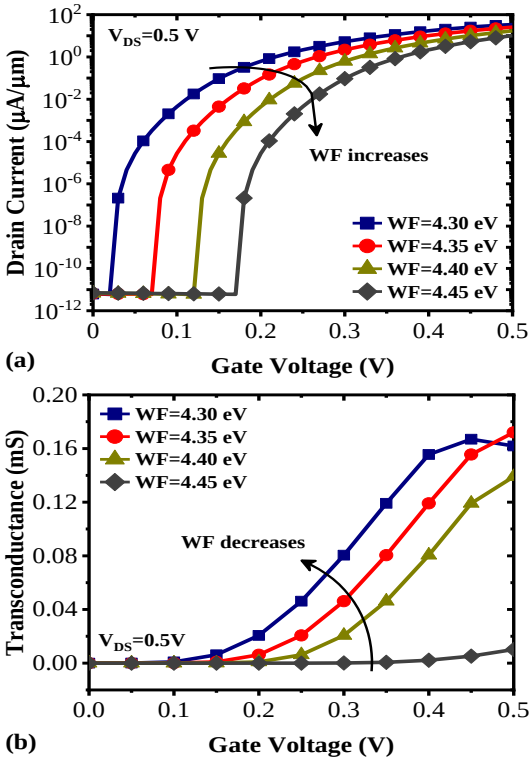

Fig. 8. Impact of the gate work function on (a) transfer characteristics, and (b) transconductance of CSNT-TFET.

Fig. 8(a) shows the effect of gate work- function on CSNT-TFET transmission characteristics. Selecting the appropriate gate work-function results in enough electric field flux at the tunneling junction, which decreases the onset voltage and increases the drain current. In this device, with increasing gate work- function from 4.3eV to 4.45eV, onset voltage increases from V_{GS} = 0.02V to V_{GS} = 0.17V.

Fig. 8(b) shows the impact of gate work-function on the transconductance of CSNT-TFET. Transconductance is given by $g_m = \partial I_D / \partial V_{GS}$ and, it is clear that lower gate work-function leads to a higher transconductance which is due to the impact of lower gate work-function on the decrement of the onset voltage (the gate voltage at which BTBT starts).

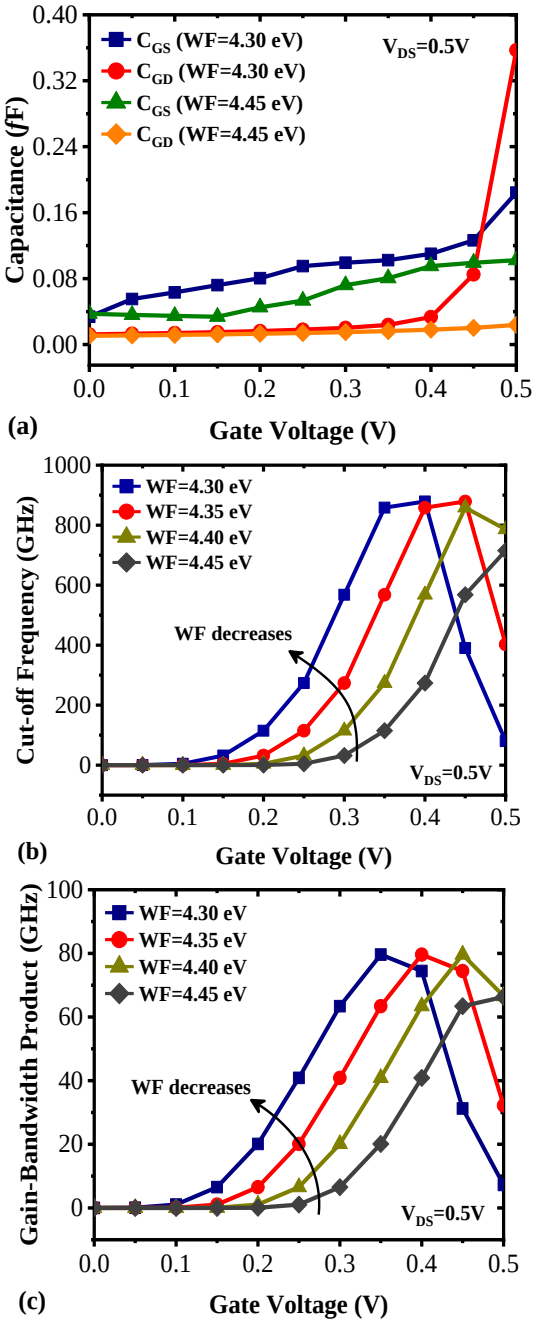

Fig. 9. Impact of the gate workfunction on (a) parasitic capacitance, (b) cut-off frequency, and (c) gain-bandwidth product of CSNT-TFET.

Fig. 9(a) examines the effect of gate work- function on CSNT-TFET parasitic capacitances. These parasitic capacitances have a great effect on the speed of the transistor, so it is better to design a device with fewer parasitic capacitances. Parasitic capacitance is composed of two main components: gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}).

From Fig. 9(a), it can be inferred that lower gate work-function leads to a higher C_{GS} and C_{GD}. This is because the lower gate work-function leads to a sharper band diagram at the tunneling junction, so we have more charge carriers on the source side of the transistor that results in higher C_{GS}. Then these charge carriers move toward the drain side of the transistor so, C_{GD} also increases.

The cut-off frequency and gain-bandwidth product are two crucial parameters of field-effect transistors. Cut-off frequency and gain-bandwidth product are defined by $f_T = g_m/2\pi(C_{GD}+C_{GS})$ and $GBW = g_m/2\pi(10C_{GD})$ respectively. From Fig. 9(b) and 9(c), it can be concluded that lower gate work function leads to a higher f_T and *GBW*. Thus we can understand that transconductance is the predominant component of parasitic capacitances. It should be mentioned that we have peak f_T and *GBW* of 878.95 GHz and 79.61 GHz for wf=4.35 eV.

In Table II and Table III, we compare the DC and AC/RF performance of our device with some similar structures. From tabs, 2 It can be inferred that our proposed device performs well at low voltage, and I_{on}/I_{off} has a reasonable value even in the presence of TAT. Table III also indicates that CSNT-TFET has a superior AC/RF performance concerning the other works.

TABLE II
Performance Comparison of Different TFET Architectures

Ref	SS_{min} (mV/dec)	SS_{avg} (mV/dec)	I_{on}/I_{off}	I_{on} (μA/μm)	V_{Bias} (V)
[13]	~18	-	$\rangle 10^{10}$	~0.01	1.0
[14]	~5	51	1.6×10^{8}	1.38	0.3
[15]	-	31.38	8.46×10^{11}	16.9	1.0
[16]	34	-	$\rangle 10^{6}$	18	1.0
[21]	10	32.01	3.92×10^{7}	52.19	0.5
[This work]	2	21.15	8.26×10^{8} (TAT included)	97.85	0.5

TABLE III
Comparison of Analog/RF Performance Of Different TFETS

Ref	V_{Bias} (V)	g_m (mS)	f_T (GHz)	*GBW* (GHz)
[21]	0.5	0.118	50.4	41.18
[22]	0.7	0.16	89.31	25.84
[23]	0.6	300	~75	~10
[24]	0.5	0.75	97.6	-
[25]	1.0	0.005	45	7.0
[26]	1.4	0.45	70	8.0
This Work	0.5	0.166	878.95	79.61

IV. Conclusion

In this article, we propose a CSNT-TFET that uses an n^+ pocket between the source and channel regions. Using this n^+ pocket along with the heterojunction improves the performance of the device and makes it a suitable candidate for low-power applications. We also showed that our proposed structure is

fully compatible with CMOS technology. All numerical simulations have been performed with the Silvaco Atlas, and the effect of nonidealities such as traps has been investigated for a fair comparison. Among the main parameters of the device, we can mention to I_{on}=97.85 µA/µm, SS_{avg}=21.15 mV/dec.

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