Design of Novel 2:4 Decoder Circuits for Quantum-dot Cellular Automata Technology

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***Abstract*--Quantum-dot Cellular Automata (QCA) technology is a highly promising emerging technology that serves as a viable alternative to CMOS technology. On the other hand, the decoder is one of the vital building blocks in digital circuits. This paper presents and evaluates two novel 2:4 decoder circuits in QCA technology. The 2:4 decoder is a crucial component in digital systems, responsible for translating binary information from encoded input signals to a unique output signal. The first proposed circuit is implemented in a single layer, and the second proposed circuit is implemented in 3 layers. The functionality of the proposed decoder circuits is verified using the QCADesigner tool. The obtained results demonstrate that the designed coplanar QCA decoder has 34 cells, 0.02 μm^2 area, and 0.5 clock cycles delay. In addition, our proposed multilayer decoder has 34 cells, 0.01 μm^2 area, and 0.5 clock cycle delay. The coplanar and multilayer developed decoder circuits have 2.08 meV and 2.33 meV, average Ebath energy, respectively. The comparison results indicate that the proposed circuits have advantages compared to other decoder circuits.**

***Index Terms*-- Nanoelectronics; Nanotechnology; QCA technology; Quantum computing; Digital circuit.**

I. INTRODUCTION

Quantum-dot Cellular Automata (QCA) technology, which was first introduced by Lent et al. [1, 2], superior to conventional CMOS technology, such as having a faster switching speed, being more stable on smaller scales, and lower power consumption. This efficiency is crucial in the development of QCA-based systems, where the reduction of hardware complexity is essential for practical implementation and scalability. So, several promising circuit designs have been presented, such as full adder circuits [3-5], comparator circuits [6, 7], multiplexer circuits [8-11], memory circuits [12, 13], multiplier circuits [14, 15], decoder circuits [16-18], ALUs [19-21] and FPGAs [22].

On the other hand, the decoder is a fundamental combinational logic circuit in digital electronics that translates binary information from encoded input signals to a unique output signal.

This paper presents and evaluates new QCA 2:4 decoder circuits. In these circuits, the design subject is minimizing both the number of cells and the occupied area. The proposed 2:4 decoder circuits in this paper are designed using four 3-input majority gates and inverters. The functionality of the proposed QCA 2:4 decoder circuits is verified using the QCADesigner tool. The results demonstrate that the proposed coplanar 2:4 decoder has 34 cells, 0.02 μm^2 area, and 0.5 clock cycle delay. In addition, the proposed three-layer 2:4 decoder has 34 cells, 0.01 μm^2 area, and 0.5 clock cycle delay.

Compared to other existing works, the advantage of our proposed 2:4 decoder circuit is that the presented single-layer circuit occupies less area. Furthermore, in the three-layer circuit presented, the occupied area is significantly reduced, and the cost is greatly improved.

This paper is organized as follows: Section II includes the background on the QCA circuit, illustrating QCA cells, clocking, and basic QCA gates. Section III presents the proposed decoder structures. Section IV discusses the implementation results and compares the proposed structures with other existing works. Finally, section V provides the conclusion.

II. BACKGROUND

A. QCA cell

The QCA cell serves as the fundamental unit of this technology, comprising four quantum dots (holes) occupied by two free electrons. According to Coulomb's law, the repulsive forces between the electrons compel them to adopt configurations that maximize their separation within a cell. So, there are only two stable states [3], as illustrated in Fig. 1.

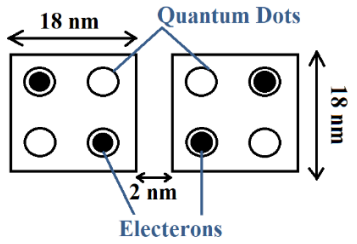

Fig. 1 . Two polarizations of the QCA cell

The polarization of each cell can influence adjacent cells, allowing us to expand and control the final polarization and the output of the circuit.

B. QCA Wire

A wire in the QCA technology is formed by the arrangement of multiple QCA cells positioned nearby, as shown in Fig. 2. In the QCA technology, there are two types of wires, (a) coplanar crossing wires and (b) multilayer crossing wires. The coplanar crossing wire is implemented in a single layer and consists of vertical and horizontal wires, while the multilayer crossing wire

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utilizes three layers for the design of crossovers, as shown in Fig. 3.

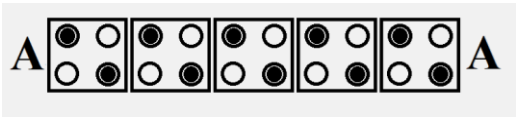

Fig. 2 . The QCA wire

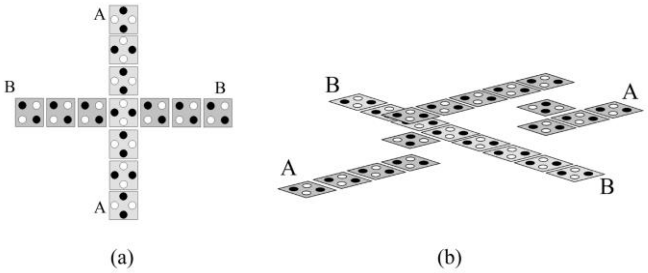

Fig. 3. Two types of wiring: (a)coplanar wiring and (b)multilayer wiring

C. QCA Gates

The most fundamental gates in the QCA technology, which form the basis of all circuits, are the Majority Voter Gates (MVGs) and the Inverter Gate (IG), as shown in Fig. 4. The IG displayed in Fig. 4 (b) has more stability compared to the IG displayed in Fig. 4 (a), whereas the IG in Fig. 4 (a) takes up less space, resulting in lower costs.

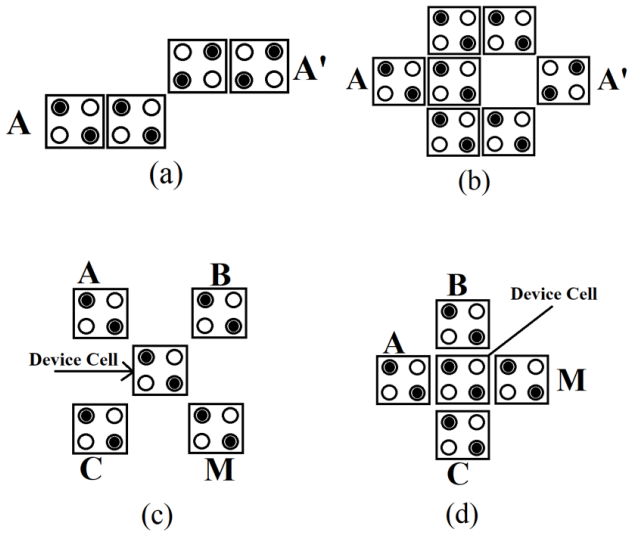

Fig. 4. Fundamental gates: (a) simple IG, (b) robust IG, (c) RMVG, (d) OMVG

Typical MVGs have three inputs and one output. The MVGs can be categorized into two types: Rotate Majority Voter Gates (RMVG) and Original Majority Voter Gates (OMVG), which are displayed in Fig. 4 (c) and Fig. 4 (d), respectively. Assuming that MVG has inputs named A, B, and C, the MVG will perform the following operation.

$$MVG(A, B, C) = AB + BC + CA \quad (1)$$

D. QCA Clocking

The clocking mechanism inherent in the QCA technology is essential for the synchronization and management of data flow among QCA cells. Fig. 5 determines the clocking scheme in the QCA technology.

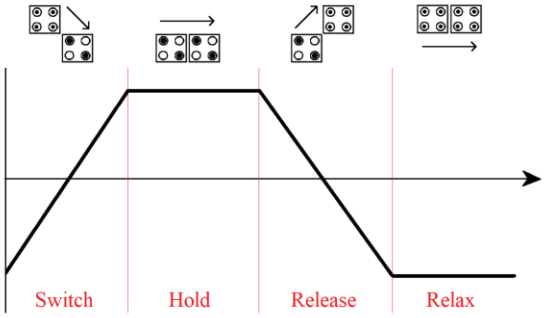

Fig. 5. The clocking scheme in QCA

Each complete clock cycle is comprised of four critical phases that influence cellular behavior as follows:

- Switch phase: Cells initially exist in an unpolarized state, which allows them to adapt to the most significant polarization affecting them.
- Hold phase: the subsequent phase involves locking in the polarization achieved during the switch phase, facilitating its transfer to neighboring cells while preemptively avoiding undesirable disturbances.
- Release phase: This phase focuses on reducing the potential barrier between electrons, allowing them to escape their constrained positions.
- Relax phase: in this concluding phase, the potential barrier reaches its lowest threshold, enabling electrons to navigate freely and conform to the prevailing polarization around them.

E. Decoder circuit

A decoder is a fundamental combinational logic circuit in digital electronics that translates binary information from encoded input signals to a unique output signal. Specifically, it takes an n-bit binary number as input and generates one of 2^n outputs corresponding to the binary value. For instance, a 2:4 decoder receives a two-bit binary input and activates one of four outputs based on the encoded value. This capability makes decoders essential components in various digital applications. The truth table of the 2:4 decoder is given in TABLE I.

TABLE I
Truth Table of 2:4 Qca Decoder

inputs		outputs			
A	**B**	**D0**	**D1**	**D2**	**D3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

F. Related works

There are several attempts [17, 23-26] to improve the performance of the QCA decoder circuit. Makanda and Jeon

[25] have proposed two 2:4 decoder circuits in a single layer, which is displayed in Fig. 6 (a) and (b). In the first circuit in Fig. 6 (a), 110 QCA cells covering an area of 0.13 μm^2 are used which has four gates and three clock phases delay. In the second circuit in Fig. 6 (b), 159 QCA cells covering an area of 0.19 μm^2 is used, which also has four gates and three clock phases delay. Mukherjee et al. [23] have presented a multilayer 2:4 decoder circuit, which is displayed in Fig. 6 (c). They utilized four 3-input MVGs and four IGs in their design. This architecture consists of 36 QCA cells covering an area of 0.01 μm^2. Zhou et al. [26] have presented a coplanar 2:4 decoder, which is displayed in Fig. 6 (d). This circuit iuses139 QCA cells, occupying 0.16 μm^2 which uses six gates and five clock phases delay. De et al. [24] have proposed a 2:4 decoder in a single layer using four 3-input MVGs and four IGs, which is displayed in Fig. 6 (e). Their work consists of 93 QCA cells and takes 0.09 μm^2 of area. Pourtajabadi and Nayeri [17] have presented a multilayer 2:4 decoder circuit, which is displayed in Fig. 6 (f). Their work consists of 100 QCA cells and takes 0.08 μm^2 area.

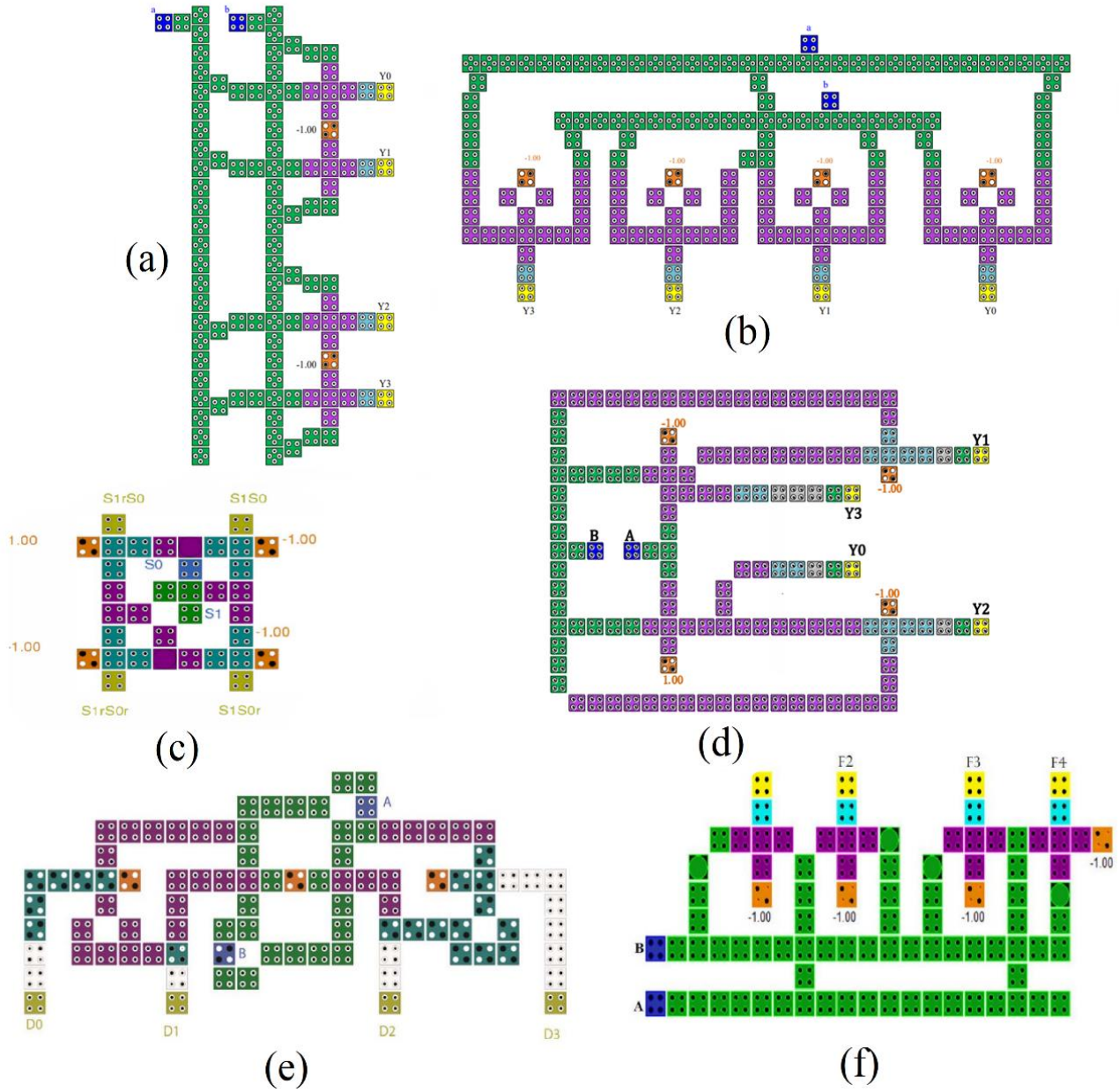

Fig. 6. The QCA decoder utilized in (a) [25] design1, (b) [25] design2, (c) [23], (d) [26], (e) [24], (f) [17]

III. THE PROPOSED 2:4 DECODER

This section presents a novel circuit for a coplanar 2:4 decoder, followed by a novel multilayer 2:4 decoder.

G. The proposed coplanar 2:4 decoder

Fig. 7 illustrates the block diagram of the proposed 2:4 QCA decoder.

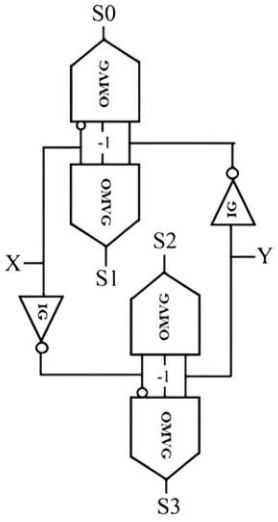

Fig. 7. The block diagram of the proposed coplanar 2:4 decoder

The outputs of the proposed 2:4 decoder are computed as follows for inputs x and y.

$$\begin{aligned} s_0 &= \bar{x}\bar{y} \\ s_1 &= x\bar{y} \\ s_2 &= \bar{x}y \\ s_3 &= xy \end{aligned} \tag{2}$$

This design consists of four majority gates and IGs. Fig. 8 illustrates the QCA layout of the designed coplanar 2:4 decoder, which has 34 cells and 0.02 μm^2 area. This QCA layout is based on the block diagram presented in Fig. 7 and Equation (2).

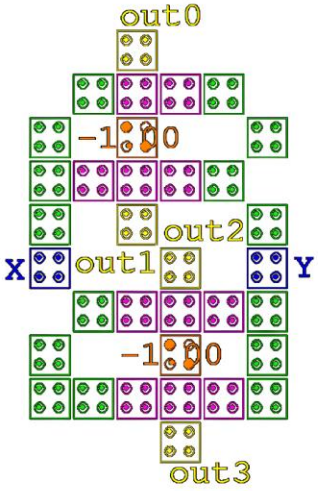

Fig. 8. The QCA layout of the proposed coplanar 2:4 decoder

H. The proposed multilayer 2:4 decoder

Fig. 9 illustrates the QCA layout of the proposed multilayer 2:4 decoder. This QCA layout is based on the block diagram presented in Fig. 7 and Equation (2).

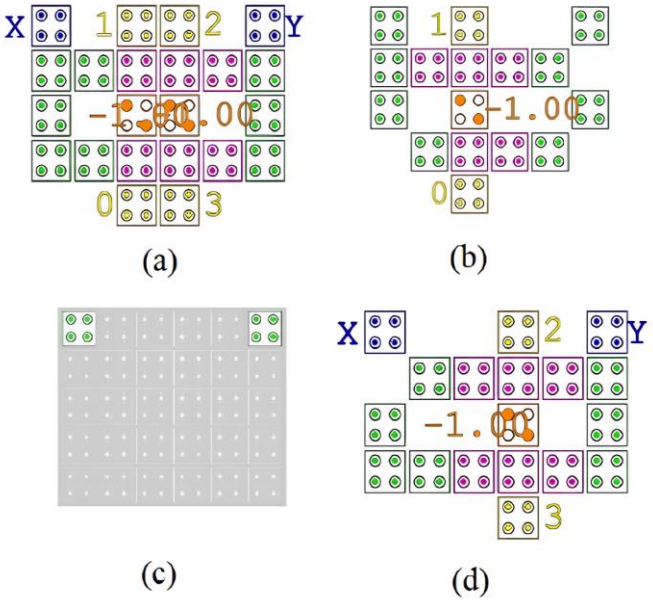

Fig. 9. The proposed multilayer 2:4 decoder a) all three layers, b)1st layer, c) 2nd layer, d) 3rd layer

Fig. 9 (a) depicts the proposed multilayer circuit, while Fig. 9 (b) shows the first layer of the designed multilayer circuit, and Fig. 9 (c) and Fig. 9 (d) illustrate the second and third layers, respectively. The design consists of 34 QCA cells, which occupies 0.01 μm^2 area.

IV. SIMULATION RESULTS AND COMPARISON

The proposed circuits are simulated and evaluated using the QCADesigner tool version 2.0.3, and the precision of its operation is demonstrated. The simulation results of the proposed coplanar and multilayer 2:4 decoder circuits are shown in Fig. *10* and Fig. *11*, respectively.

TABLEII summarizes and compares the simulation results of the proposed 2:4 decoder circuit with other similar works. In this table, CLA, COM, TLA, CLK, LAT, and AUG indicate cell area, complexity (cell count), total area, total clock phases, latency (total clock cycles), and area usage, respectively. In addition, ADC, ALC, and CTL are calculated as follows.

$$\begin{aligned} &ADC = Area \times Delay^2 \\ &ALC = Area \times Latency \\ &CTL = COM \times TLA \times LAT \end{aligned} \tag{3}$$

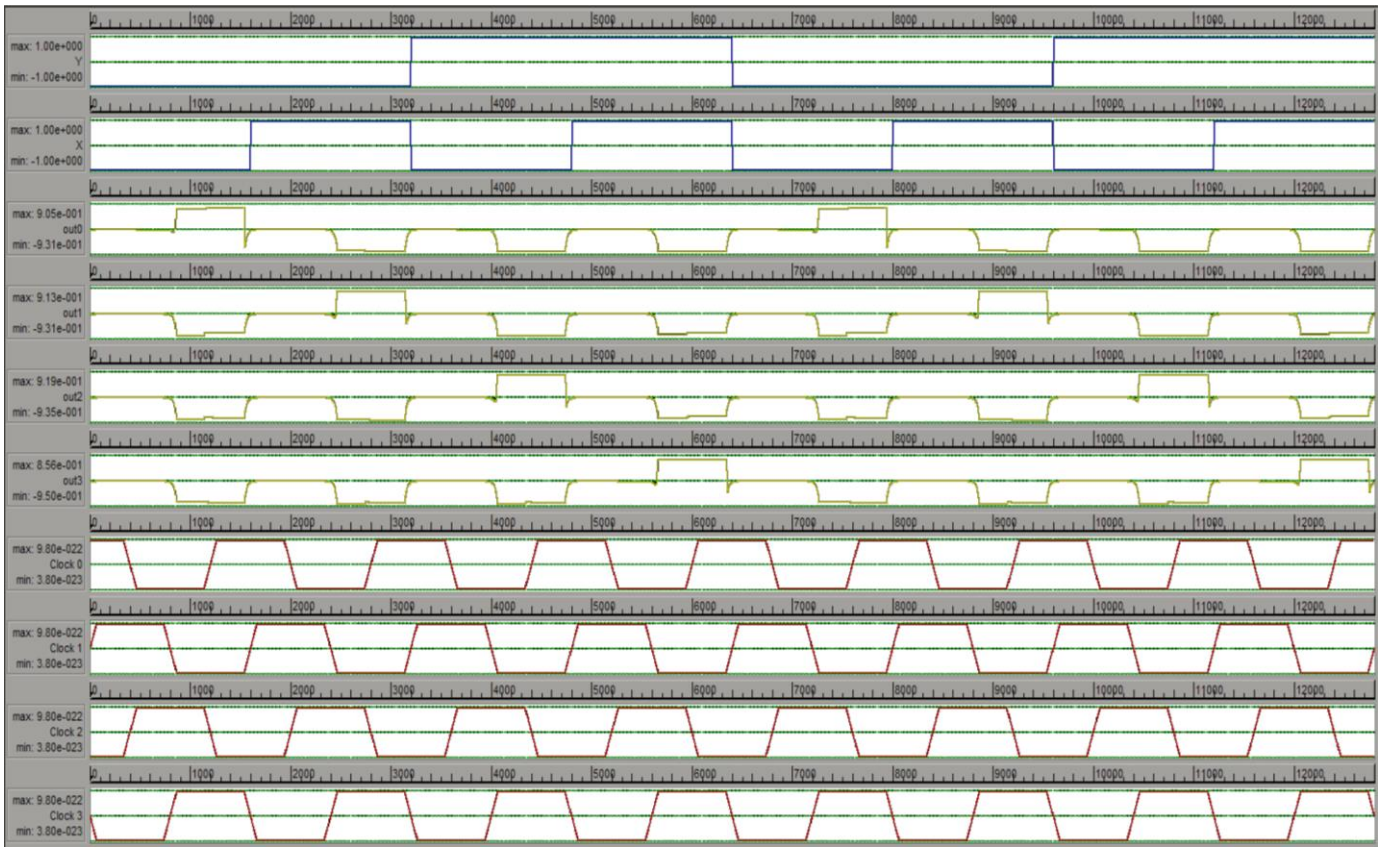

Fig. 10. Simulation result for the proposed coplanar design

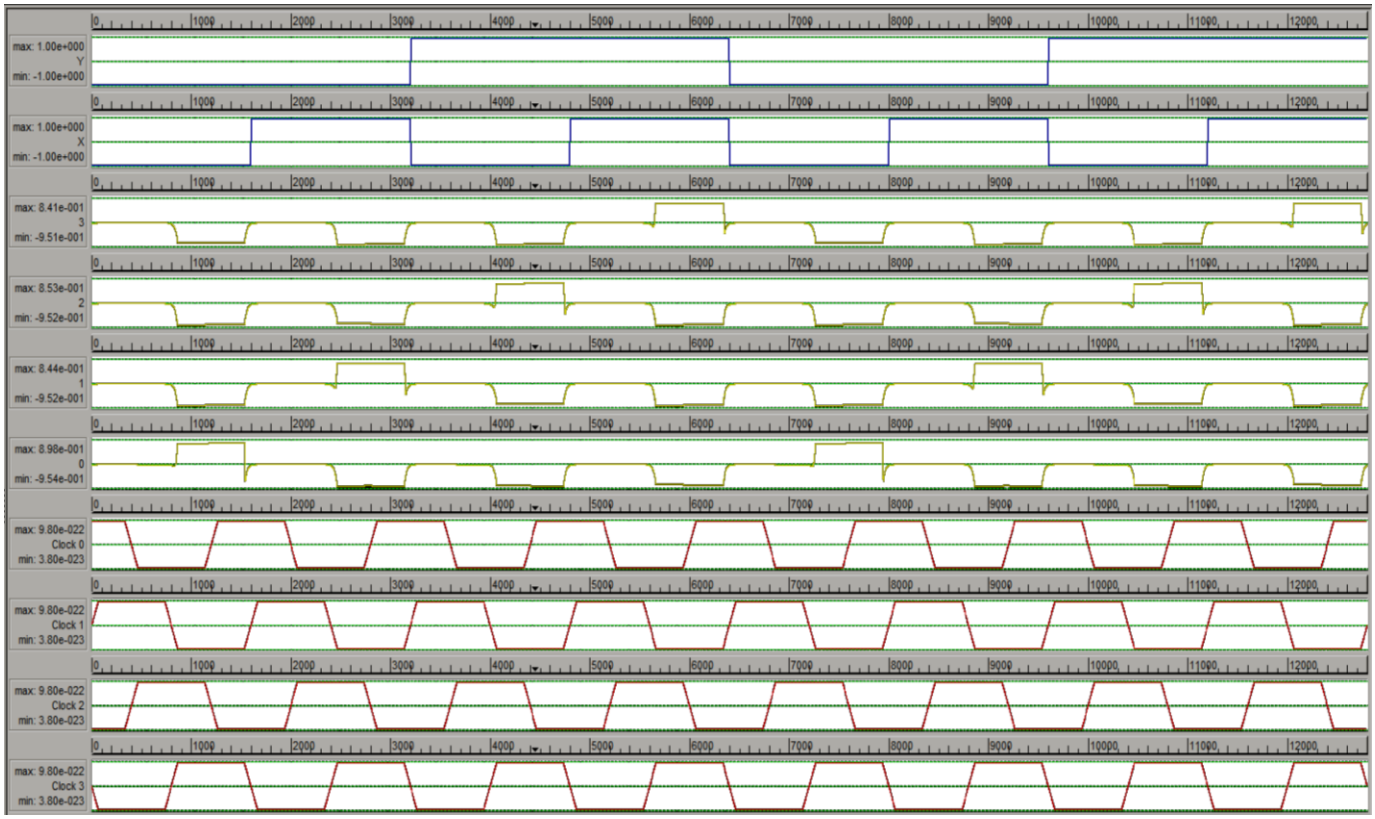

Fig. 11. Simulation result for the proposed multilayer design

TABLE II
Comparison Results

Reference	COM	CLA (μm^2)	TLA (μm^2)	LAT	CLK	Crossover	ALC	ADC	CTL
[23]	36	0.0117	0.012	0.75	3	multilayer	0.009	0.108	0.324
[24]	93	0.0301	0.09	0.5	2	coplanar	0.045	0.36	4.185
[25] circuit 1	110	0.0356	0.13	0.75	3	coplanar	0.0975	1.17	10.725
[25] circuit 2	159	0.0515	0.19	0.75	3	coplanar	0.1425	1.71	22.6575
[26]	139	0.0450	0.16	1.25	5	coplanar	0.2	4	27.8
[17]	100	0.0324	0.08	0.75	3	multilayer	0.06	0.72	6
This paper, coplanar circuit	34	0.0110	0.02	0.5	2	coplanar	0.01	0.08	0.34
This paper, multilayer circuit	34	0.0110	0.01	0.5	2	multilayer	0.005	0.04	0.17

TABLE III and TABLE IV summarize the performance improvement in terms of TLA, ALC, ADC, and CTL for coplanar and multilayer 2:4 decoder, respectively. In these tables, the improvement of the suggested circuits is calculated as follows.

$$\text{Improvement (\%)} = \left(1 - \frac{new\ cost}{old\ cost}\right) \times 100 \quad (4)$$

TABLE III
Comparison Table for 2:4 Coplanar Decoder Circuit

Reference	TLA (μm^2)	ALC	ADC	CTL
[24]	78%	78%	78%	92%
[25] circuit 1	85%	90%	93%	97%
[25] circuit 2	90%	93%	95%	98%
[26]	87.5%	95%	98%	99%

TABLE IV
Comparison Table for 2:4 Multilayer Decoder Circuit

Reference	TLA	ALC	ADC	CTL
[23]	17%	45%	63%	48%
[17]	87.5%	92%	95%	97%

The proposed coplanar 2:4 decoder circuit has advantages compared to coplanar 2:4 decoder circuits in [24-26] in terms of the TLA, ALC, ADC, and CTL by about 78%-90%, 78%-95%, 78%-98%, and 92%- 99%, respectively. For example, the developed coplanar 2:4 decoder circuit has 87.5%, 95%, 98%, and 99% improvements compared to the presented work in [26] in terms of the TLA, ALC, ADC, and CTL, respectively.

The proposed multilayer 2:4 decoder circuit has advantages compared to multilayer comparator circuits in [17, 23] in terms of the TLA, ALC, ADC, and CTL by about 17% - 87.5%, 45% - 92%, 63%- 95%, and 48%-97%, respectively. For example, the developed multilayer 2:4 decoder circuit has 87.5%, 92%, 95%, and 97% improvements compared to the presented work in [17] in terms of TLA, ALC, ADC, and CTL, respectively.

The energy consumption of QCA circuits is estimated using QCADesigner-E [27, 28]. TABLE V compares the results of the presented 2:4 decoder circuits using the Coherence Vector (w / Energy) simulation engine of QCADesigner-E. The utilized parameters for the simulation are the default settings. The power dissipation of a circuit is calculated as follows [19].

$$P_d = E_d / T \quad (5)$$

Where P_d is the power dissipation, Ed is the average dissipated energy in Joules, and T is the total time taken to create the output. ($Ed = Avg\_Ebath \times 1.602 \times 10^{-19}$)

The estimated energy and power consumption of the proposed 2:4 decoder circuits is lower than the decoder circuits in [17, 25, 26], demonstrating the enhanced energy efficiency of the designed circuits in this paper. This improvement in energy performance highlights the advantages of the proposed circuit implementation over previously reported 2:4 decoder circuits.

TABLE V
Estimated Energy for the Proposed 2:4 Decoder Circuits

Reference	***Sum_Ebath*** **(meV)**	***Avg_Ebath*** **(meV)**	***Error_Sum_Ebath*** **(meV)**	***Error_Avg_Ebath*** **(meV)**	***Power consumption*** **(*μW*)**
[25] circuit 1	37.2	3.38	-3.07	-0.279	4.51
[25] circuit 2	40.1	3.64	-2.98	-0.271	4.86
[26]	45.2	4.11	-3.79	-0.345	3.29
[17]	27.2	2.48	-2.17	-0.197	3.31
This paper, coplanar circuit	22.9	2.08	-2.34	-0.212	4.17
This paper, multilayer circuit	25.6	2.33	-2.62	-0.238	4.67

V. Conclusion

The QCA technology is a promising substitute for CMOS technology for creating digital circuits in Nanoscale. The decoder circuit is a useful and versatile instrument for executing logical combinations. This paper presents and evaluates novel coplanar and multilayer 2:4 decoder circuits in the QCA technology. The developed circuits were simulated using QCADesigner tool version 2.0.3. Additionally, the energy estimation of the circuits was determined using QCADesigner-E, an extension made for calculating the energy dissipation of circuits. Based on the results, both decoder circuits had advantages compared to similar works in terms of occupied area, delay, energy consumption, ALC, ADC, CTL, and power consumption.

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