Modeling of Drain Current in Double-Gate Heterojunction Tunneling FETs: a Physical-Analytical Approach

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***Abstract*— In this paper, we develop an analytical potential model for the double-gate Heterostructure Tunneling Field-Effect Transistors (H-TFETs) to accurately predict the electrostatic potential profile of the device in all regions of operation. Using the potential model, we present appropriate relations for the tunneling distance at a specified energy level in the bandgap of the tunneling junction. Finally, based on the highest tunneling rate formalism, the minimum tunneling distance is employed to calculate the tunneling current, which is the dominant on-state current flow mechanism in the H-TFETs. We show that our models closely match the results obtained by numerical simulations, for various heterostructure devices with different material systems in a wide range of operation, from subthreshold to super threshold..**

***Index Terms*— Analytical modeling, band-to-band tunneling, double-gate heterostructure tunnel field-effect transistor (H-TFET), Drain Current.**

I. Introduction

Utilization of proper heterojunctions to form the tunneling junction of the tunneling field effect transistors (TFETs) has increased the drive current, decreased the subthreshold current, and improved the switching characteristics of the device. Pursuing superior device performance, researchers have studied various material systems and introduced some promising combinations such as InGaAs-InP [1, 2], InAs-Si [3, 4], InAs-AlGaSb [5], and SiGe-Si [6] heterojunctions.

In spite of the extensive lab experiments and numerical simulations, physical and analytical models accurately predicting the characteristics of the heterojunction TFETs (H-TFETs) are in the beginning stages of development. Complexity of physical and analytical modeling of H-TFETs has obliged researchers to simplify the problem and inevitably admit some inaccuracy in the model results in some regions of device operation. For example reported models in [7–12] do not seem to work accurately at high gate biases, because they have completely neglected the influence of mobile carriers in the channel of H-TFET on the electrostatics of the device. On the other hand, overestimation of the tunneling current is expected when the model ignores any energy band bending in the reservoirs [8, 10, 13]. Models developed in [7, 11] are based on the assumption that the channel can be divided to two depleted and non-depleted regions, regardless of bias condition. It can be easily shown that for a short channel device or a device with low gate biases such a division is not generally reasonable. In [14], we presented an accurate physical model for the drain current of double-gate H-TFETs. Our modeling approach was based on integrating the band to band tunneling (BTBT) generation rate over the tunneling volume which requires several simplifying assumptions to lead to an analytical, but not compact, expression predicting the drain current. In [15], we achieved a model for the tunneling distance at the given energy level in the tunneling window, which leads us to develop a closed-from drain current model introduced in the current paper.

In this paper, a physical and analytical approach is taken to develop an appropriate model for the drain current of the heterostructure double gate TFET devices. The utilized potential profile model includes band bending in the source and drain regions, and takes into account modulation by the mobile carriers in the channel at super threshold operation region. Based on our potential model, a model for the drain current of the device is derived and validated for all operation regions of H-TFETs. The rest of the paper is organized as follows. In Section 2, our model for the potential profile in the H-TFET is developed. In Section 3, a model for the drain current is introduced. The results of the developed models are verified by those obtained from a numerical device simulator for different set of parameters and material systems in section 4, while section 5 concludes the paper.

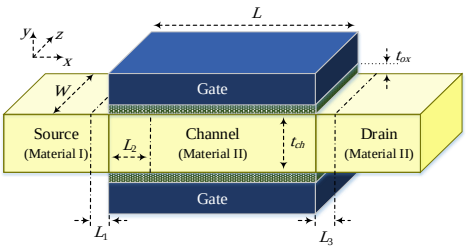

Fig. 1. A schematic 3D view of a double gate heterojunction TFET. The coordinate system, the device dimensional parameters and the extensions of the depletion regions in the source, channel and drain regions are also depicted.

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II. Potential Model Derivation

A schematic 3D view of a symmetric double gate heterojunction TFET is shown in Fig. 1, where tox, tch, L, and W stand for the gate oxide thickness, channel thickness, channel length, and channel width, respectively. L1, L2, and L3 are the bias-dependent lengths of the depletion region extensions in the source, channel and drain, respectively. Such a separation helps us use more reasonable simplifications which are inevitable when one is going to deal with physical equations analytically. Consequently, a more accurate analytical model for the potential profile along the device is expected. The oxide layer can be a single layer insulator or a composition of two stacked layers of a high-k dielectric and a dielectric that provides a better interface at the junction with the channel material [9, 16].

A. Potential profile around the tunneling junction

The tunneling rate of carriers is highly sensitive to the band bending around the tunneling junction. Part of this bending occurs in the source depletion region, especially at higher gate voltages, and the other part occurs in the channel depletion region. Since the electrostatic potential distribution in a wide channel device ($W >> L$) is almost independent of the z coordinate, we seek the 2-D profile for the potential in the channel depletion region which is obtained from the following equation

$$\frac{\partial^2\varphi_{c1}(x,y)}{\partial x^2}+\frac{\partial^2\varphi_{c1}(x,y)}{\partial y^2}=-\frac{qN_{ch}}{\varepsilon_{ch}} \tag{1}$$

where $\varphi_{c1}(x,y)$ is the electrostatic potential, N_{ch} is the doping concentration of the channel region, and ε_{ch} is the permittivity of the channel material. Owing to the symmetry of the structure the boundary conditions in y-direction can be stated as

$$\left.\frac{\partial\varphi_{c1}(x,y)}{\partial y}\right|_{y=\frac{t_{ch}}{2}}=0$$
$$C_{ox}[V_{GS}-\varphi_{mch}-\varphi_{s1}(x)]=-\varepsilon_{ch}\left.\frac{\partial\varphi_{c1}(x,y)}{\partial y}\right|_{y=0} \tag{2}$$

where, C_{ox} is the oxide capacitance, φ_{mch} is the work function difference between the gate material and the channel, and φ_{s1} is the surface potential. We approximate the potential profile in y direction by the second-order polynomial ($\varphi_{c1}(x,y) = \varphi_{s1}(x)+ C_1(x).y+ C_2(x).y^2$), and substitute it in the Poisson's equation of (1) (considering the boundary conditions of (2)). This yields a second order differential equation for the surface potential,

$$\frac{\partial^2\varphi_{s1}(x)}{\partial x^2}-\frac{1}{\lambda_{ch}^2}\varphi_{s1}(x)=-\frac{qN_{ch}}{\varepsilon_{ch}}-\frac{1}{\lambda_{ch}^2}(V_{GS}-\varphi_{mch}) \tag{3}$$

where, $\lambda_{ch}=(\varepsilon_{ch}t_{ch}/2C_{ox})^{0.5}$.

At the left end of this region, $x = 0$, the surface potential approaches φ_{S0} which is the surface potential at the source-channel interface, and at the right end, $x = L_2$, it is assumed that the lateral field fades to zero and $\varphi_{s1}(L_2)$ can be obtained from the 1-D Poisson's equation in vertical direction. The solution of this equation is reported in [17].

Having these boundary conditions, the linear differential equation of (3) can be solved analytically as,

$$\varphi_{s1}(x)=\varphi_{\perp ch}-\left(\varphi_{\perp ch}-\varphi_{s1}(L_2)\right)\cosh\left(\frac{x-L_2}{\lambda_{ch}}\right) \tag{4}$$

where, $\varphi_{\perp ch}=V_{GS}-\varphi_{mch}-qN_{ch}t_{ch}/2C_{ox}$.

Considering the gate fringing field, the same 2-D Poisson's equation governs the potential profile in the depletion region of source and the same approach as that of the channel region is utilized to find the surface potential profile in this region. The solution is:

$$\varphi_{ss}(x)=\varphi_{\perp s}-(\varphi_{\perp s}+V_{bi})\cosh\left(\frac{x+L_1}{\lambda_s}\right) \tag{5}$$

where, $\varphi_{\perp s}=V_{GS}-\varphi_{ms}-qN_st_{ch}/2C_{fr}$, $\lambda_s=(\varepsilon_s t_{ch}/2C_{fr})^{0.5}$ and the built-in potential is given by:

$$V_{bi}=\chi_s-\chi_{ch}+\frac{E_{g-s}-E_{g-ch}}{2}+\frac{kT}{q}ln\left(\frac{N_sN_{ch}}{n_{is}n_{ich}}\right) \tag{6}$$

In the above relations, φ_{ms} is the work function difference between the gate material and the source, N_s, ε_s, χ_s, $E_{g\text{-}s}$, and n_{is} are the doping concentration of acceptors, the permittivity, the electron affinity, the energy bandgap, and the intrinsic carrier concentration of the source region, respectively, and χ_{ch}, $E_{g\text{-}ch}$, and n_{ich} are the electron affinity, the energy bandgap, and the intrinsic carrier concentration of the channel region, respectively. All energies are expressed in electron volts. C_{fr} is the fringing capacitance which is introduced as $C_{fr} \approx 2/\pi\ C_{ox}$ [18].

From the continuity of the potential and the electric displacement field at the source-channel interface, the following explicit relations for L_1 and L_2 are obtained,

$$L_1=\lambda_s cosh^{-1}\left(\frac{\eta K+\sqrt{(1-K)(1-K/\gamma^2)+\eta^2K}}{1-K}\right)$$
$$L_2=\lambda_{ch}cosh^{-1}\left(\frac{\eta\gamma-\sqrt{(1-K)(\gamma^2-K)+\gamma^2\eta^2K}}{1-K}\right) \tag{7}$$

where, $K=\varepsilon_{ch}C_{ox}/\varepsilon_sC_{fr}$,

$$\gamma=\frac{\varphi_{\perp s}+V_{bi}}{\varphi_{\perp ch}-\varphi_{s2}(L_2)}\ \text{ and }\ \eta=\frac{\varphi_{\perp ch}-\varphi_{\perp s}}{\varphi_{\perp s}+V_{bi}}\ .$$

Focusing on the results obtained from the potential model developed above, it can be inferred that as the gate voltage decreases L_2 increases, and even may extend beyond the channel length. In such circumstances, dividing the channel area into the depleted and non-depleted regions with clear boundary is pointless. Here we introduce a new definition for the boundary that restricts the amount of extension of the depletion region in the channel. According to this definition, the border between these two regions in the channel is specified using a specific non-zero lateral electric field (E_{bor}), such that if L_2 (calculated from (7)) exceeds the channel length, the new location for the boundary is calculated as:

$$L_{2-new}=L_2-\lambda_{ch}asinh\left(\frac{\lambda_{ch}E_{bor}}{\varphi_{s2}(L_2)-\varphi_{\perp ch}}\right) \tag{8}$$

On the other hand, at the lower gate voltages in which the device is practically in the off-state, the above model leads to a negative lateral electric field in the channel depletion region which is not acceptable for an n-channel device in its normal

operation mode. To avoid such a condition the term $\varphi_{\perp ch} - \varphi_{s2}(L_2)$in (5) should always remain greater than zero, requiring that:

$$V_{GS} > \varphi_{mch} - qN_{ch}t_{ch}/2C_{ox} + \varphi_{s1}(L_2) \quad (9)$$

Indeed, the above inequality is violated when the whole channel of the device is completely depleted from the charge carriers. Hence, we provide a new presentation for the channel surface potential,

$$\varphi_{s1}(x) = \varphi_{\perp ch} + I_1 exp\left(\frac{x-L}{\lambda_{ch}}\right) + J_1 exp\left(-\frac{x}{\lambda_{ch}}\right) \quad (10)$$

where the coefficients I_1 and J_1 can be determined from the continuity of the potential at the left and right end of the channel as,

$$I_1 = \frac{\varphi_{D0} - \delta\varphi_{S0} - (1-\delta)\varphi_{\perp ch}}{1-\delta^2}$$
$$J_1 = \frac{\varphi_{S0} - \delta\varphi_{D0} - (1-\delta)\varphi_{\perp ch}}{1-\delta^2} \quad (11)$$

In (11), φ_{D0} is the surface potential at the drain-channel interface, and δ = exp(-L/λ_{ch}). φ_{S0} and φ_{D0} will be determined later from the continuity of the electric displacement vector (electric field) at the source-channel (channel-drain) interface.

B. Potential profile in the channel non-depleted region

In the non-depleted region of the channel, we include mobile charge carriers in the 2-D Poisson's equation.

$$\frac{\partial^2\varphi_{c2}}{\partial x^2} + \frac{\partial^2\varphi_{c2}}{\partial y^2} = \frac{qn_{ich}}{\varepsilon_{ch}} exp\left(\frac{\varphi_{c2} - V_{DS}}{kT/q}\right) \quad (12)$$

where V_{DS} is substituted for the quasi Fermi level in this part [14], and the small doping density of the intrinsic channel is neglected against the charge carriers' density. In [14] the same equation is solved using the superposition principle. That is, the electrostatic potential is written as the sum of two terms:

$$\varphi_{c2}(x,y) = \varphi_{1D}(y) + \varphi_{2D}(x,y) \quad (13)$$

where $\varphi_{1D}(y)$ is the solution of the 1-D Poisson's equation and $\varphi_{2D}(x,y)$ is the solution of the residual 2-D differential equation. The solution of the 1-D potential term is obtained as [17]:

$$\varphi_{1D} = V_{DS} - \frac{2kT}{q} ln\left(\frac{t_{ch}}{2\beta}\sqrt{\frac{q^2 n_{ich}}{2\varepsilon_{ch}kT}} cos\left(\frac{2\beta}{t_{ch}}y - \beta\right)\right) \quad (14)$$

where β can be calculated from the following relation,

$$\frac{q(V_{GS} - \varphi_{mch} - V_{DS})}{2kT} + ln\left(\frac{t_{ch}}{2}\sqrt{\frac{q^2 n_{ich}}{2\varepsilon_{ch}kT}}\right) = ln(\beta) - ln(cos\beta) + \frac{2\varepsilon_{ch}}{t_{ch}C_{ox}}\beta tan\beta, \quad (15)$$

and the solution of the 2-D potential term is approximated as [14]:

$$\varphi_{2D}(x,y) = \left[I_0 e^{\left(2\lambda\frac{x-L}{t_{ch}}\right)} + J_0 e^{\left(-2\lambda\frac{x-L_2}{t_{ch}}\right)}\right] cos\left(\frac{2\lambda}{t_{ch}}y - \lambda\right) \quad (16)$$

where λ can be calculated from the following relation

$$\lambda \cdot \tan(\lambda) = \frac{t_{ch}C_{ox}}{2 \cdot \varepsilon_{ch}}; \quad \text{where} \quad 0 < \lambda < \frac{\pi}{2} \quad (17)$$

Several approximations for λ are given in [19]. Using the continuity of the surface potential at the left and right ends of the region, we find the unknown coefficients of φ_{2D} as:

$$I_0 = \frac{\varphi_{D0} - \varphi_{1D}(0)}{(1-\xi^2)cos\lambda}$$
$$J_0 = \frac{\xi(\varphi_{D0} - \varphi_{1D}(0))}{(\xi^2 - 1)cos\lambda} \quad (18)$$

where ξ=exp(-2λ(L-L_2)/t_{ch}).

It should be noted that the model developed in this subsection is only applicable when the bias condition meets the inequality of (9), otherwise there exists essentially no non-depleted region in the channel. When $L_{2\text{-}new}$, is employed, the original relations need no modification, only $\varphi_{1D}(0)$ in equation (18) should be replaced with $\varphi_{s1}(L_{2\text{-new}})$.

C. Potential profile in the drain depletion region

Usually to suppress the ambipolar behavior in TFETs, the drain region closed to the channel is not heavily doped [20], so the extension of the depletion region in the drain is non-negligible especially in the subthreshold operation regime. Ignoring the variation of the potential in the vertical direction, we solve the 1-D Poisson's equation inside the depletion region. At x=L+L_3 the potential and the lateral electric field reach V_{DS}+KT/q ln(N_d/N_{ch}) and zero, respectively. N_d is the doping concentration of donors in the drain. The solution of the Poisson equation gives,

$$\varphi_d(x) = -\frac{qN_d}{2\varepsilon_{ch}}[x - (L + L_3)]^2 + V_{DS} + \frac{kT}{q} ln\left(\frac{N_d}{N_{ch}}\right) \quad (19)$$

On the other side, the potential and the electric field are continuous at the drain-channel interface. Employing these conditions leads to the following relation for φ_{D0},

$$\varphi_{D0} = \varphi_{1D}(0) - \frac{H^2}{2} + \sqrt{\left(\varphi_{1D}(0) - \frac{H^2}{2}\right)^2 - \varphi_{1D}^2(0) + H^2\left(V_{DS} + \frac{kT}{q} ln\left(\frac{N_d}{N_{ch}}\right)\right)} \quad (20)$$

where,

$$H = \frac{1-\xi^2}{1+\xi^2}\frac{t_{ch}}{2\lambda}\sqrt{\frac{2qN_d}{\varepsilon_{ch}}}.$$

Furthermore, since $\varphi_d(L) = \varphi_{D0}$, the length of the depletion region in drain, L_3, can explicitly be expressed.

Note that $\varphi_{1D}(0)$ in equation (20) is replaced with $\varphi_{s1}(L_{2\text{-new}})$, if $L_{2\text{-new}}$ is taken into account. Furthermore, for the lower gate voltages in which the inequality of (9) is not satisfied, the boundary conditions at the drain-channel junction lead a system of nonlinear equations for φ_{S0} and φ_{D0} as shown in (21). Having these values, we can obtain L_1 and L_3 from (5) and (19), respectively.

III. Drain Current Model

BTBT is the dominant current flow mechanism in TFETs. Drain current calculation in TFETs requires integrating the tunneling generation rate over the tunneling volume around the tunneling junction. One method to find this current is based on the highest tunneling rate ($G_{t\text{-}max}$), given by:

$$\begin{cases} \dfrac{\sqrt{K}}{(\varphi_{\perp s}+V_{bi})}\left\{\dfrac{2\delta\varphi_{D0}-(1+\delta^2)\varphi_{S0}+(1-\delta)^2\varphi_{\perp ch}}{1-\delta^2}\right\}=\sqrt{\left(\dfrac{\varphi_{\perp s}-\varphi_{S0}}{\varphi_{\perp s}+V_{bi}}\right)^2-1} \\ \dfrac{1}{\lambda_{ch}}\left\{\dfrac{(1+\delta^2)\varphi_{D0}-2\delta\varphi_{S0}-(1-\delta)^2\varphi_{\perp ch}}{1-\delta^2}\right\}=\sqrt{\dfrac{2qN_d}{\varepsilon_{ch}}\left(V_{DS}+\dfrac{kT}{q}ln\left(\dfrac{N_d}{N_{ch}}\right)-\varphi_{D0}\right)} \end{cases} \quad (21)$$

$$I_{DS}=2q\cdot G_{t-max}\cdot\lambda_{tun}\cdot W\cdot t_{ch}\cdot f_{fermi} \quad (22)$$

where λ_{tun} is a material-dependent tunneling decay length that depends on the effective band gap (E_{g-eff}) and the effective tunneling mass of the carriers [7]. In an n-type device, the effective band gap is the energy difference between the source valence band and the channel conduction band at the source-channel interface. f_{fermi} is a correction factor which is defined to avoid non-zero current at V_{DS}=0V as [21],

$$f_{fermi}=2\cdot\left[\frac{1}{2}-\frac{1}{\left(1+\exp\left(\frac{qV_{DS}}{f_n kT}\right)\right)}\right]. \quad (23)$$

The maximum tunneling rate, G_{t-max} occurs in the minimum tunneling distance (D_{t-min}) and is formulated by Kane as [22],

$$G_{t-max}=A\frac{E_{g-eff}^{\frac{3}{2}}}{q^2}\cdot\frac{1}{D_{t-min}^2}\exp\left(-\frac{D_{t-min}}{\lambda_{tun}}\right). \quad (24)$$

A is a material-dependent parameter of the Kane's model. Our potential model provides a closed form relation for the tunneling distance for a carrier with a given energy E. Whether the inequality of (9) is satisfied or not, the tunneling distance is calculated from (25) or (26), respectively. It should be noted that the unit of energies in these relations is electron volts. Substituting the source Fermi energy level in these relations, one can obtain D_{t-min}.

In the subthreshold region of operation, the tunneling generation rate is negligible and the dominant charge transport mechanism is p-i-n diode reverse bias leakage current (I_S) [14]. In [23], this current is formulated as (27), where D_P and D_N are the diffusion coefficients, τ_P and τ_N are the hole and electron lifetimes, respectively, and W_N and W_P are the lengths of the drain and source regions, respectively. It should be noted that the contribution of the trap-assisted tunneling in the subthreshold conduction is not considered in this work.

IV. Results and Discussion

In this section, we validate our models' predictions for the potential profile and the drain current against the results obtained from a numerical device simulator [24]. The comparison is carried out for different device dimensions, applied biases, and the oxide and heterojunction material systems. The default quantities for the device parameters are L = 50nm, t_{ch} = 10nm, and t_{ox} = 2nm (composed of 1nm of SiO_2 and 1nm HfO_2), N_s = 10^{20}, N_d = 10^{19} cm^{-3}, and the work function of the gate material is 4.5eV.

The surface potential profile along the channel of a double gate InGaAs-InP H-TFET with an applied drain voltage of 1V is shown in Fig. 2. The model results, which are validated by the simulation results, confirm that the depletion regions lengths inside the source and drain are evidently bias dependent. It should be noted that, based on the extensive simulations carried out on the different structures at different bias conditions, E_{bor} is set to 1MV/m, which is two orders of magnitude less than the maximum electric field at the source-channel interface. As mentioned before, this value is used to increase the validity of the model for low gate voltages and short channel lengths, where L_2 exceeds the channel length. The inset shows the accuracy of our potential model predictions for different oxides, where SiO_2, Si_3N_4 and HfO_2 are employed in various structures. The potential profiles from the proposed model show good agreement with the results obtained from the numerical simulations.

In Fig. 3 the electrostatic potential distributions for an InAs-Si H-TFET with an applied drain voltage of 0.5V, are plotted for different gate biases. This heterojunction has an staggered band alignment which leads to a high tunneling current for the device [9]. As shown in the figure, our model can predict the simulation results with very good accuracy. The same plots are illustrated in the inset for an InAs-AlGaSb H-TFET, where we indicate the validity of the model results for different values of the drain-source applied voltages. InAs-AlGaSb H-TFET is another example of a TFET with high drive current [5].

$$D_t(E)=L_1+L_2-\lambda_s acosh\left(\frac{\varphi_{\perp s}-E}{\varphi_{\perp s}+V_{bi}}\right)-\lambda_{ch}acosh\left(\frac{\varphi_{\perp ch}-(E+E_{g-eff})}{\varphi_{\perp ch}-\varphi_{s1}(L_2)}\right) \quad (25)$$

$$D_t(E)=L_1-\lambda_s acosh\left(\frac{\varphi_{\perp s}-E}{\varphi_{\perp s}+V_{bi}}\right)+\lambda_{ch}ln\left(\frac{E+E_{g-eff}-\varphi_{\perp ch}+\sqrt{\left(E+E_{g-eff}-\varphi_{\perp ch}\right)^2-4I_1J_1\delta}}{2I_1\delta}\right) \quad (26)$$

$$I_S=qt_s\left(\frac{n_{i2}^2}{N_d}\sqrt{\frac{D_P}{\tau_P}}coth\left(\frac{W_N-L_2}{\sqrt{\tau_P D_P}}\right)+\frac{n_{i1}^2}{N_s}\sqrt{\frac{D_N}{\tau_N}}coth\left(\frac{W_P-L_1}{\sqrt{\tau_N D_N}}\right)\right) \quad (27)$$

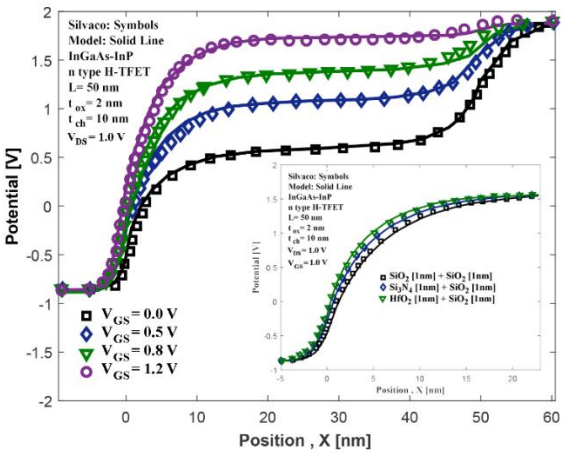

Fig. 2. Surface potential profile of an n type InGaAs-InP H-TFET along the device obtained from the model (symbols) and numerical simulation (lines). Inset: the same profile for different oxide structures of SiO_2/SiO_2, Si_3N_4/SiO_2, and HfO_2/SiO_2. The drain bias is 1V and the gate bias is used as running parameter. Device dimensional parameters are depicted in the figure. The channel region is located between 0 and 50nm.

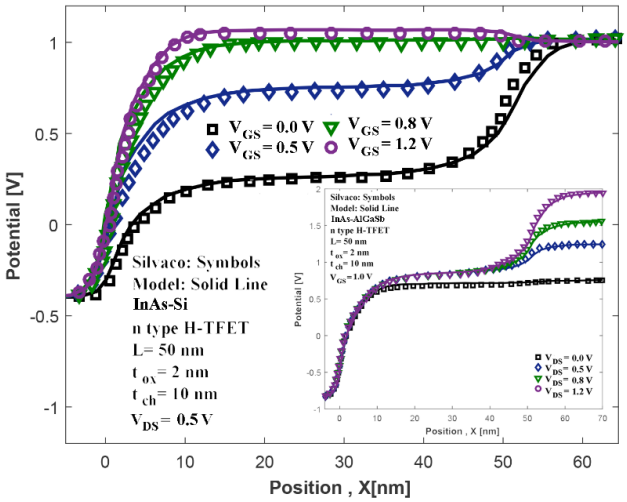

Fig. 3. Surface potential profile of an InAs-Si H-TFET along the device obtained from the model (symbols) and simulation (lines). Inset: Surface potential profile of an InAs-AlGaSb H-TFET along the device for different values of V_{DS} applied voltages.

Fig. 4 shows the transfer characteristic of an InAs-Si H-TFET in logarithmic scale with two different channel lengths at V_{DS}=1V. As it can be inferred from this figure, the channel length does not considerably modulate the drive current in TFETs. The characteristics plotted in the figure using numerical simulation validate the accuracy of our drain current model for an H-TFET based on the InAs-Si heterojunction. The accuracy of the drain current model for two InAs-Si and InGaAs-InP H-TFETs with different gate dielectric materials is investigated in Fig. 5, where various

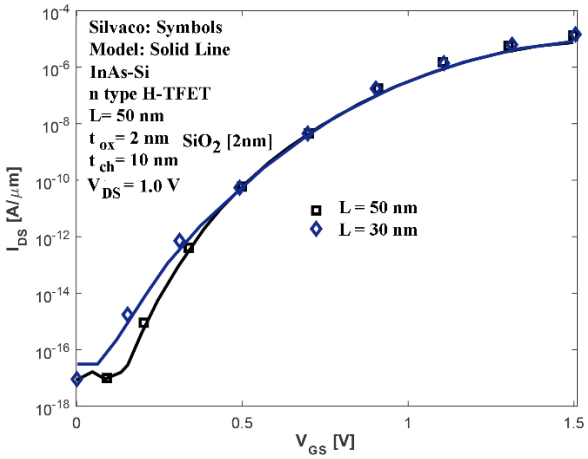

Fig. 4. log(I_{DS})-V_{GS} curves predicted by numerical simulation (lines) and by the analytical model (symbols) for an InAs-Si H-TFET with two different lengths of the channel and t_{ox}=3nm, t_{ch}=10nm, and V_{DS}=1V.

combinations of SiO_2, HfO_2 and Si_3N_4 are employed. In all cases, the gate dielectric thickness is assumed to be 2nm. As expected, improved electrostatic coupling between the gate and the tunneling junction is achieved by the gate dielectric with higher effective permittivity which leads to a higher drive current, steeper subthreshold slope, and higher I_{ON}/I_{OFF} current ratio.

Fig. 6 shows the influence of the drain bias on the I_{DS}-V_G characteristics of an InGaAs-InP H-TFET. For a short channel TFET both the drain and the gate biases can modulate the tunneling distance and consequently the on-state current. It is accurately predicted by our proposed drain current model. Finally, we investigate the conformity of the model predictions to the simulation results through the output characteristics of several H-TFETs based on different heterojunction material systems given in Fig. 7. The inset shows one of these curves at V_{GS}=1V.

V. Conclusion

In this paper, a potential model predicting the electrostatic profile for the heterostructure tunnel field-effect transistors is developed which is applicable from the subthreshold to the super threshold regime. The modeled potential profile takes into account the band bending in the source and drain regions, and the modulation by the mobile carriers' density in the channel at super threshold region. Our analytical potential model led us to introduce analytical expressions for the tunneling distance in the bandgap of the tunneling junction. We employed the minimum tunneling distance and calculated the drain current of the device using highest tunneling rate formalism. By comparing results obtained from our model with those obtained from the numerical device simulator, we validated the predictions of the potential and the current models for the various heterostructure devices with different material systems in all regions of operation.

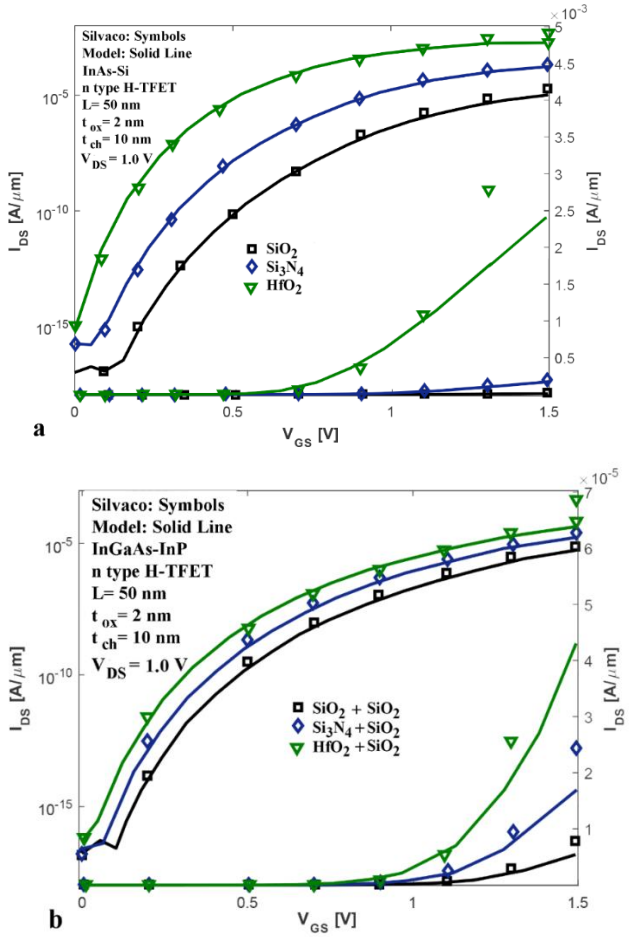

Fig. 5. log(I_{DS})-V_{GS} curves of (a) InAs-Si H-TFET and (b) InGaAs-InP H-TFET predicted by numerical simulation and by the model for various gate dielectrics, SiO_2 (ε_{ox}=3.9), Si_3N_4 (ε_{ox}=7.5), and HfO_2 (ε_{ox}=21).

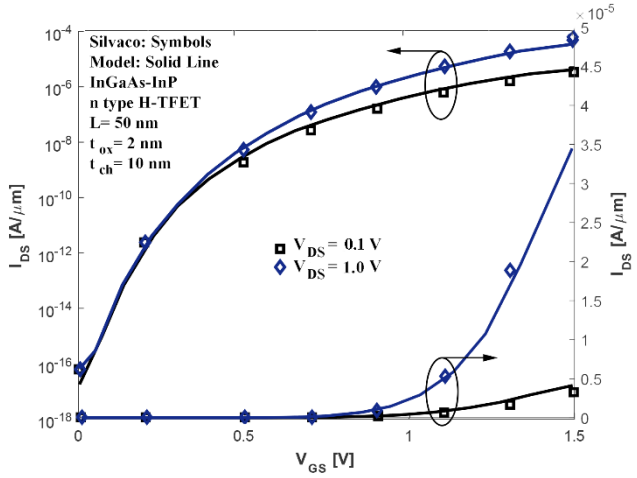

Fig. 6. log(I_{DS})-V_{GS} characteristics of the InGaAs-InP H-TFET for two different drain voltages predicted by numerical simulations (lines) and by analytical model (symbols). The other parameters are t_{ox}=2nm, t_{ch}=10nm, L=50nm, and V_{DS}=1V.

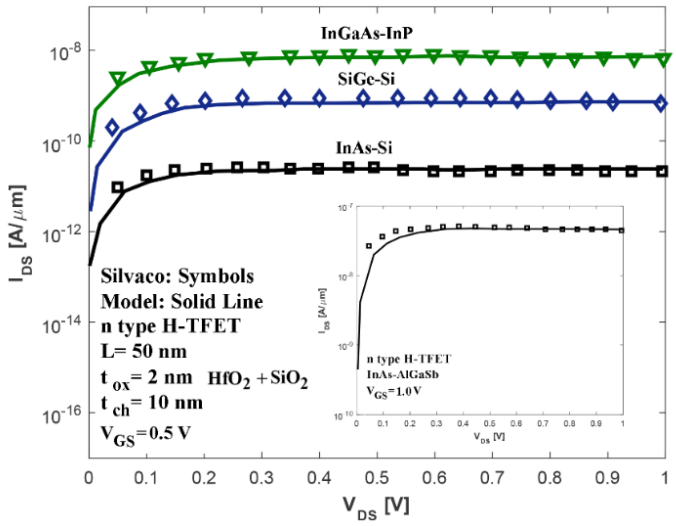

Fig. 7. log(I_{DS})-V_{DS} characteristics for several H-TFETs based on different material systems predicted by numerical simulation (lines) and by analytical model (symbols).

VI. References

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