A Modified High Voltage Gain Switched-Capacitor-Inductor Active-Switched Boost Inverter

Zahra Mokhtari[1] and Amin Asghari[2]

***Abstract*-- This article proposes a new controller for a switched-capacitor-inductor-active switched boost inverter (SCL-ASBI). The proposed controller provides a high voltage gain. This controller improves the boost factor without adding extra components to the SCL-ASB inverter. This control method increases the boost factor with a low duty cycle, and paves the way for the soft-switching condition of the switches. The control method has the shoot-through (ST) state to reduce electromagnetic interference (EMI) noises. The boost factor is flexible, owing to utilizing a phase shift in this method. The switching algorithm and theoretical analysis are discussed. The simulation results are presented to confirm the validity of the theoretical analysis and the advantages of the proposed inverter.**

***Index Terms*--single-stage inverter, switched-capacitor-inductor, soft switch, controller, impedance network**

I. INTRODUCTION

IN the past few years, scientists focused on single-stage power inverters (SSIs) that convert DC input voltage into AC output voltage. SSIs have low weight, low cost, high reliability, and high performance [1].

The Z source inverter (ZSI) is introduced in [2]-[5]. In ZSI, DC-line is connected to the H-bridge via two capacitors and two inductors. Despite the advantages, such as operating in buck or boost and ST modes, there exist plenty of elements.

The quasi-Z-source inverter (qZSI) is a reasonable option in renewable energy applications [6], [7] due to having continuous input current, boosting capability, and capacitor voltage stress. The qZSI has Shoot Through state (ST). In the ST state, both switches in one leg are on. This feature can increase the voltage gain. Also, the reliability is enhanced because dead-time is not required. The qZSI is suitable for photovoltaic (PV) systems and electric vehicles [8]-[12]. Despite the mentioned advantages, its practical boosting ability is not enough.

To achieve a high gain, several structures based on Z-source inverter and (quasi-) Z-source inverter have been introduced in [13]-[21], In these structures, high gain is achieved by adding extra inductors, capacitors, and diodes. In Diode-assisted quasi-switched Z-impedance network is proposed in [29]. This ZSI and capacitor-assisted quasi-ZSI introduced in [15], the voltage gain is improved. However, these structures are complex. By adding a switched inductor (SL) in ZSI/qZSI, boosting is increased [16], [17]. Ripple input current SL-qZSI and continuous input current SL-qZSI, enhanced-boost z-source inverter based on switched z-impedance, and Enhanced-boost quasi Z-source inverters with two switched impedance networks (EB-qZSI) are respectively introduced in [18]-[20]. All these topologies involve many passive elements, which increase volume and cost.

The switched-capacitor inductor qZSI can suppress inrush current at the start-up moment [21]. The switched-capacitor inductor ZSI with an impedance network can be cascaded and has low voltage stress [22]. the qZSI with combined two quasi-Z-source networks has a common ground between the input source and the inverter bridge and low voltage stress across the switches [23]. The switched inductor/capacitor quasi Z-source inverter has low voltage stress and low input current ripple [24]. These topologies pay off with improving boost factor in spite of involving many passive components. It is not a trivial matter.

The active-switched structures are proposed to improve the boost factor. In these topologies, by adding a few elements, the output voltage is increased more than other extended boost Z-source inverters. In the conventional active switched inverter, the active switch is on in the ST mode and is off in the non-ST mode. The drawback of the active-switched structures is that a separate gate driver is needed for the additional switch [25].

The structures that increase the boost factor by adding extra inductors, capacitors, and diodes to the qZSI topology are presented in [26]-[30]. The extended boost active-switched-capacitor/switched-inductor qZSI (CSC-EB-ZSI) is proposed in [26]. The enhanced-boost qZSI with an active switched Z-network (EB/ASN-qZSI) is introduced in [27]. The inverters proposed in [20], [26], and [27] have the same boosting, while the number of LC pairs in [26] is reduced. The conventional active-switched inductor boost qZSI (cASLB-qZSI) [28] provides continuous input current and higher boost voltage than [26] and [27]. The high boost non-isolated qZSI with an active inverter has the common ground between the bridge inverter

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and the input voltage source, lower current stress. Also, this inverter can suppress the inrush startup current. The high voltage gain active switched qZSI (HGAS-qZSI) is presented in [30]. The boost factor of [30] is improved. However, the number of components in the Z-source network increases.

The switched boost inverter (SBI) and the embedded-type quasi-switched boost inverter (qSBI) are presented in [31], [32]. The high voltage gain quasi-switched boost inverter (HG-qSBI) is presented in [33]. Although the input current is continuous and has a low ripple, the boost factor is not high enough. The enhanced boost-quasi Z source inverter is introduced in [34]. This inverter can improve the boost factor and reduce the number of inductors. In embedded-type qSBI, although the number of elements is equal to SBI, the voltage gain increases. A high gain-switched capacitor-quasi switched boost inverter (HG-SC-qSBI) was proposed in [35]. In this topology, the boost factor is high, but the number of elements is increased.

A capacitor-inductor active-switched boost inverter (SCL-ASBI) based on the SBI structure is introduced in [36]. The introduced SCL-ASBI has few elements compared with other SBIs.

This paper introduces a new controller for SCL-ASBI. The SCL-ASBI offers higher boost ability with low number of elements in the impedance network. The advantages of the proposed topology are high voltage gain with a low duty cycle, continuous input current, low EMI noises, and soft switching conditions. Two switches turn on in ZVS condition and two switches turn off in ZVS condition. In addition, the phase shift and ST duty ratio are two factors in the voltage gain of the proposed structure that increase flexibility. Also, SCL-ASBI can be extended to make a higher boost factor by cascading n cells, whereas one cell involves an inductor, a diode, and two capacitors. The introduced inverter is acceptable for high-frequency applications. In subsequent, firstly, SCL-ASBI is presented. Afterward, the introduces HG-SCL-ASBI and its steady-state analysis are presented. After that, the design of the passive elements is discussed. Eventually, the introduced HG-SCL-ASBI is compared with some other inverters to verify the theoretical analysis.

II. Introduced HG-SCL-ASBI

A. Switched-Capacitor-Inductor Active-Switched Boost Inverters

The SCL-ASBI topology can be seen in Fig. 1 It includes two inductors (L_1, L_2), three capacitors (C_1, C_2, and C_3), seven diodes (D_1-D_3), and five switches (S_0-S_4). By applying the proposed controller to SCL-ASBI, the boost factor is improved. In the theoretical analysis, the current of inductors and voltages of capacitors are supposed to be constant because these inductors and capacitors are large enough [36].

B. The Proposed SPWM Control method for HG-SCL-ASBI

The PWM control method are common in inverters [2], [37]. This paper proposes a new controller for SCL-ASBI that increases the boost factor. The proposed switching method uses phase shift, high-frequency carrier, and high-frequency sin wave. This switching algorithm is illustrated in Fig. 2. The triangular carrying waveform v_{tri} and the sine waveform v_{sin} shift by $\propto$ radians and made v'_{tri} and v'_{sin}. These two signals are used to generate the gate pulses of S_1-S_2.

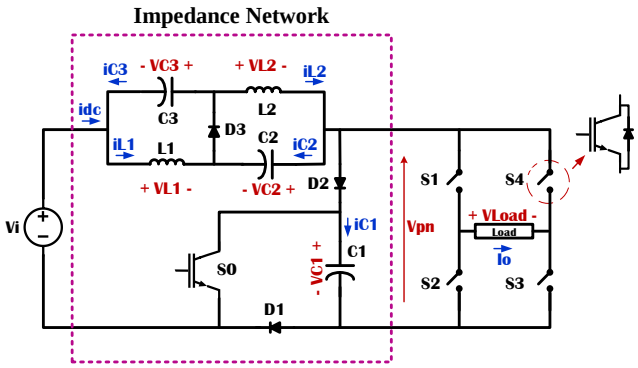

Fig. 1. HG-SCL-ASBI topology.

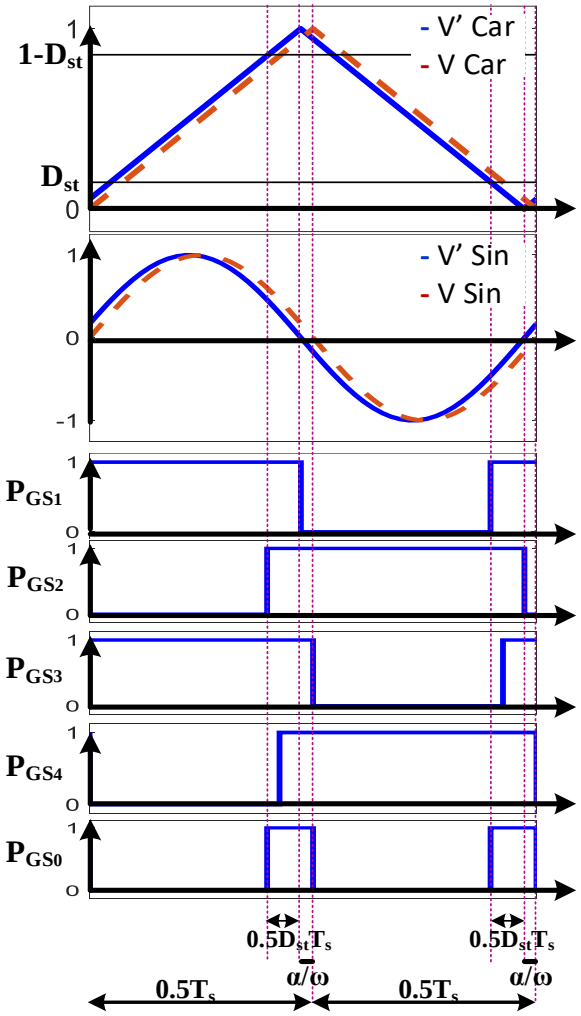

Fig. 2. The proposed SPWM controller for HG-SCL-ASBI.

The signals $u, \acute{u}, \bar{u}, \bar{u'}$ are generated as (1):

$$\begin{aligned} v_{sin} \geq 0 \rightarrow u = 1, v_{sin} < 0 \rightarrow \bar{u} = 1 \\ v'_{sin} \geq 0 \rightarrow \acute{u} = 1, v'_{sin} < 0 \rightarrow \bar{u'} = 1 \end{aligned} \quad (1)$$

D_{st} is the duty cycle of shoot-through state S_1- S_2 switches. Finally, by utilizing these two waveforms, D_{st} and 1- D_{st}, the switching pulses are generated as (2):

$$\begin{aligned} P_{GS_1} &= [(D_{ST} \geq v'_{tri}) \cap \bar{u'}] \cup \acute{u} \\ P_{GS_2} &= [(v'_{tri} \geq 1 - D_{ST}) \cap \acute{u}] \cup \bar{u'} \\ P_{GS_3} &= [(D_{ST} \geq v_{tri}) \cap \bar{u}] \cup u \\ P_{GS_4} &= [(v_{tri} \geq 1 - D_{ST}) \cap u] \cup \bar{u} \end{aligned} \quad (2)$$

In equation (2), $\cap$ is the logical and, $\cup$ is the logical or, and $P_{GS_1} - P_{GS_4}$ are the gate pulses of S_1- S_4. When $S_1$and S_2 or S_3 and S_4 are on, the switch S_0 must be on. Therefore, the gate pulse of the switch S_0 is as (3):

$$P_{GS_0} = (P_{GS_1} \cap P_{GS_2}) \cup (P_{GS_3} \cap P_{GS_4}) \quad (3)$$

Fig. 3 shows the generation of P_{GS_0} from gate pulses of S_1- S_4. The gate pulses of switches S_1- S_2 or S_3-S_4, have 180° phase differences in commonplace switching methods, in H-bridge. However, in this technique, owing to the ST state, which is indicated by $(D_{ST} + {}^{\alpha}/_{\omega})$, these two pulses overlap. Also, the S_3 and S_4 signals have $\propto$ radians phase shifts, compared to the S_1 and S_2 gate signals, respectively. This procedure enhances the boost factor and creates soft-switching in several switches.

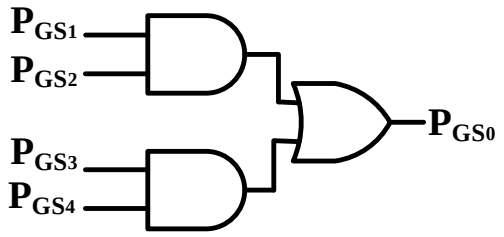

Fig. 3. Generation of P_{GS_0} from the gate pulses of S_1-S_4.

C. Operation analysis

In the proposed controller, the frequency of the sine wave and the triangular carrier is the same, and the switching cycle of the HG-SCL-ASBI is divided into eight states.

Mode 1) [$t_0 < t < t_1$]:

The first operating mode is depicted in Fig. 4(a). It starts with concurrent conduction of S_1, S_3, and D_1, D_2, D_3. However, in this mode, S_0, S_2, and S_4 are off. All capacitors C_1, C_2, and C_3 are charging. On the contrary, L_1 and L_2 are discharging.

Therefore, the voltages of L_1 and L_2, and the currents of C_2 and C_3 are written by (4)-(6):

$$L_1 \frac{di_{L1}}{dt} = -V_{C3} = Vi + V_{C2} - V_{C1} \quad (4)$$

$$\begin{aligned} L_2 \frac{di_{L2}}{dt} &= V_{C2} \\ C_2 \frac{dV_{C2}}{dt} &= i_{L2} - i_{C1} - I_O \\ C_3 \frac{dV_{C3}}{dt} &= -i_{L1} - i_{C1} - I_O \end{aligned} \quad (5)$$

$$V_{Load} = V_{Max} = V_{C1} \quad (6)$$

Mode 2) [$t_1 < t < t_2$]:

Fig. 4(b) shows the second mode. The S_1, S_2, S_3, and S_0 switches are on, where D_1, D_2, and D_3 diodes are turned Off. This type of conduction charges both inductors L_1 and L_2, whereas the capacitors C_1-C_3 are discharging during the second mode.

The results of simultaneous conduction of the S_1, S_2, and S_3 switches are zero voltage across the load, $V_{Load} = 0$, and the voltage across the S_4 switch is equivalent to zero too.

The voltages of L_1 and L_2, and the currents of C_2 and C_3 can be written by (7), (8):

$$\begin{aligned} L_1 \frac{di_{L1}}{dt} &= Vi + V_{C2} + V_{C1} \\ L_2 \frac{di_{L2}}{dt} &= Vi + V_{C3} + V_{C1} \end{aligned} \quad (7)$$

$$\begin{aligned} C_2 \frac{dV_{C2}}{dt} &= -i_{L1} = -i_{L2} - i_{C1} \\ C_3 \frac{dV_{C3}}{dt} &= -i_{L2} = -i_{L1} - i_{C1} \end{aligned} \quad (8)$$

Mode 3) [$t_2 < t < t_3$]:

The third operating mode is illustrated in Fig. 4(c). The S_4 switch is turning on ZVS in this mode, and D_1, D_2, and D_3 are turning off. Consequently, during this mode both inductors, L_1 and L_2, are charging, where the capacitors C_1-C_3 are discharging. The voltage across to the load is zero, $V_{Load} = 0$.

Thus, the voltages and currents are present in mode 2.

Mode 4) [$t_3 < t < t_4$]:

In this mode, S_0, S_2, S_3, and S_4 are on. This mode is depicted in Fig. 4(d). However, the S_1 switch is turning off ZVS, and D_1, D_2, and D_3 are turning off too. This type of conduction charges L_1 and L_2. On the contrary, C_1-C_3 are discharging. Thus, the voltages of L_1 and L_2 and the currents of C_2 and C_3 can be written as mode 2.

The results of simultaneous conduction of the S_2, S_3, and S_4 switches are $V_{Load} = 0$, and the voltage across the S_1 switch is zero.

Mode 5) [$t_4 < t < t_5$]:

Fig. 4(e) shows the fifth mode. S_2, S_4, and D_1-D_3 are conducting, whereas S_1, S_3, and S_0 are turning off. C_1-C_3 are charging, whereas L_1 and L_2 are discharging. S_2 and S_4 are simultaneous on and thus the negative output voltage is maximum as (9).

As a result, the inductors voltages and the capacitors currents equations are given in mode 1.

$$V_{Load} = -V_{Max} = -V_{C1} \quad (9)$$

Mode 6) [$t_5 < t < t_6$]

In this mode (Fig. 4(f)) the switches S_1, S_2, and S_4, are conducting, and the diodes D_1-D_3 are off. So C_1, C_2, and C_3 are discharging and L_1 and L_2 are charging. The result of conducting the S_1, S_2, and S_4 switches is $V_{Load} = 0$, and the voltage across the S_3 switch is zero.

The equations of capacitors voltages and the inductors currents are given in mode 2.

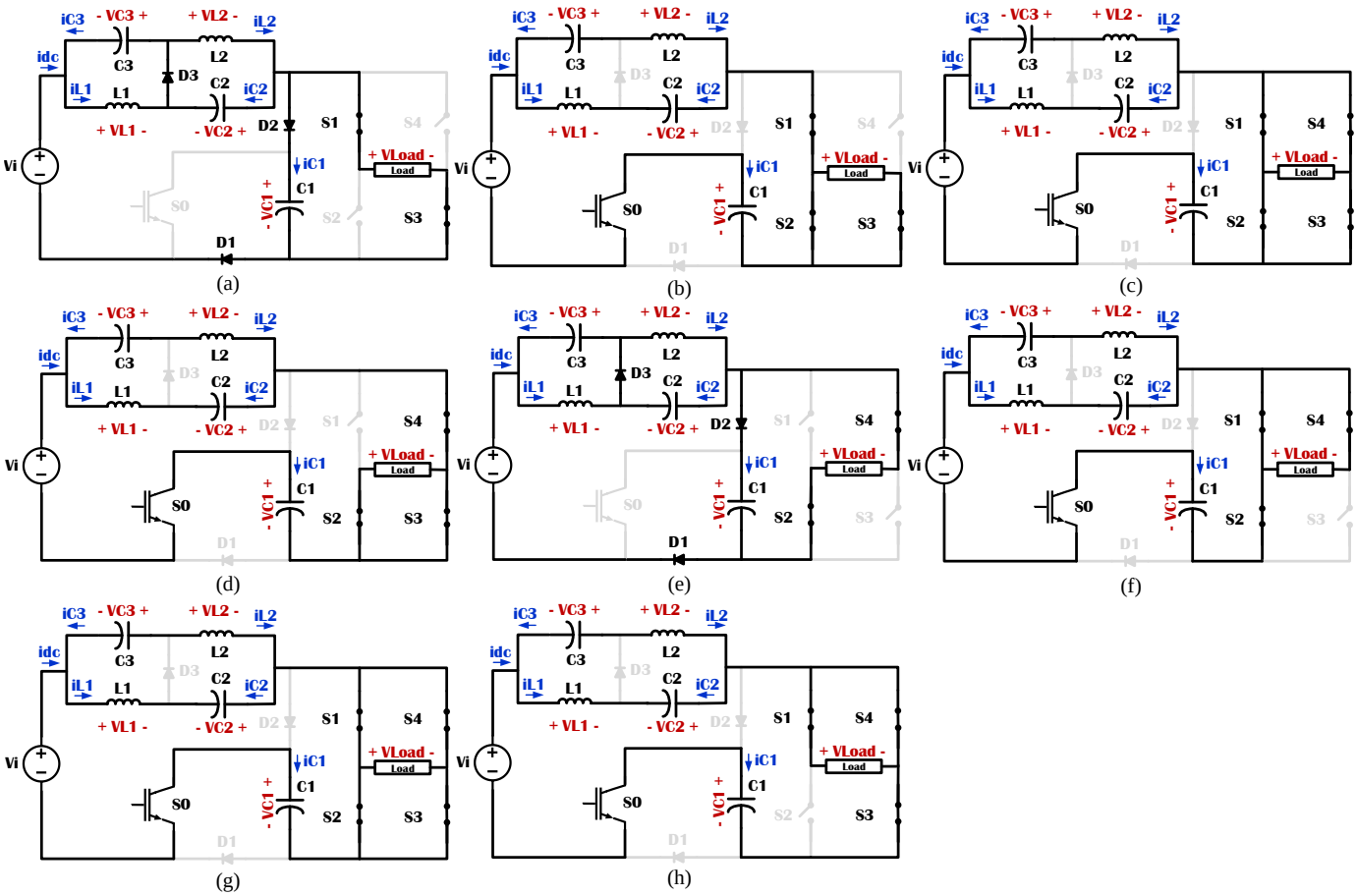

Fig. 4. Operating state of HG-SCL-ASBI. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, (h) Mode 8.

Mode 7) [$t_6 < t < t_7$]

The seventh mode is illustrated in Fig. 4(g). The S_3 switch is turning on ZVS in current mode, and D_1, D_2, and D_3 are turning off. Consequently, during this mode, both inductors L_1 and L_2 are charging, where the capacitors C_1-C_3 are discharging. The output voltage is equivalent to zero, $V_{Load} = 0$.

The voltages and currents are presented in mode 2.

Mode 8) [$t_7 < t < t_8$]

In this mode, However, S_0, S_1, S_3, and S_4 are conducted, the S_2 switch is turning off ZVS, and D_1, D_2, and D_3 are turning off too. It is shown in Fig. 4(h). This type of conduction is charging L_1 and L_2. On the contrary, C_1-C_3 are discharging. Thus, the voltages of L_1 and L_2, and the currents of C_2 and C_3 can be written as mode 2.

Simultaneous conduction of the S_1, S_3, and S_4 switches are $V_{Load} = 0$, and the voltage across the S_2 switch is zero.

In the steady-state analysis (Fig. 5), the average voltages across the inductors L_1 and L_2 and the currents through the capacitors C_1-C_3 in one switching period are zero. Utilizing voltage-Second balance during one switching period T_s, the three voltages of the capacitors are given as (10):

$$\begin{aligned} &-V_{C3}\left(1-\frac{\propto}{\pi}-D_{ST}\right)\times 0.5T+\\ &(V_i+V_{C2}+V_{C1})\times\left(D_{ST}+\frac{\propto}{\pi}\right)0.5T=0\\ &-V_{C2}\left(1-\frac{\propto}{\pi}-D_{ST}\right)\times 0.5T+\\ &(V_i+V_{C3}+V_{C1})\times\left(D_{ST}+\frac{\propto}{\pi}\right)0.5T=0 \end{aligned} \tag{10}$$

Equation (11) is obtained from (10):

$$\begin{aligned} V_{C1} &= V_i\left(\frac{1}{1-4D_{ST}-4\frac{\propto}{\pi}}\right)\\ V_{C2} &= V_{C3} = V_i\left(\frac{2D_{ST}+2\frac{\propto}{\pi}}{1-4D_{ST}-4\frac{\propto}{\pi}}\right) \end{aligned} \tag{11}$$

From (10), (11), the maximum voltage of the load in the non-ST state is expressed as (12):

$$V_{Load} = V_{C1} = V_i\left(\frac{1}{1-4D_{ST}-4\frac{\propto}{\pi}}\right) \tag{12}$$

utilizing amper–second balance point to the capacitors C_1- C_3 in one period T_s, the currents of L_1, L_2 are as (13):

$$i_{L1} = i_{L2} = \left(\frac{1-D_{ST}-\frac{\propto}{\pi}}{1-4D_{ST}-4\frac{\propto}{\pi}}\right)I_O \tag{13}$$

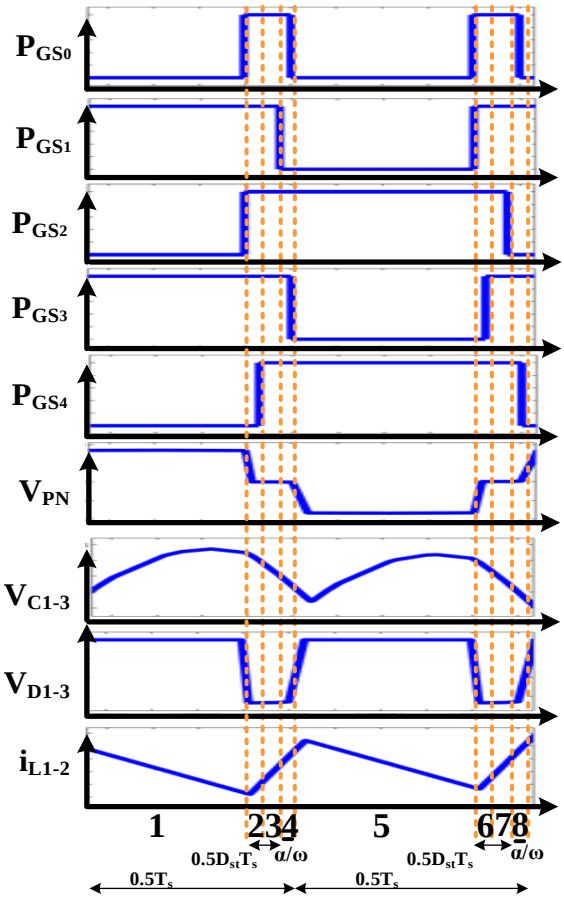

Fig. 5. Ideal waveforms of HG-SC-qSBI.

III. IMPEDANCE PARAMETER SELECTION

The HG-SCL-ASBI voltage gain is expressed as (14):

$$B = \frac{V_{Load}}{V_i} = \frac{1}{1-4D_{ST}-4\frac{\propto}{\pi}} \tag{14}$$

A. Inductance Selection

The load current, I_O, is expressed as (15):

$$I_O = \frac{V_{pn}}{R_l} \tag{15}$$

In the ST mode, the current of inductors increases, from (7), the peak-to-peak current ripple of inductors L_1 and L_2, $\Delta I_{L1,2}$ is (16):

$$\Delta I_{L1,2} = \frac{V_i+V_{C2}+V_{C1}}{L_{1,2}} \times \frac{(D+\frac{\propto}{\pi})}{2\times f_s} \tag{16}$$

f_s is the frequency of the operating point. The $r_L\%$ of inductors L_1 and L_2 is (17):

$$r_L\% = \frac{\Delta I_L}{I_{L1}} \tag{17}$$

From (11), (13), (16), and (17), the value of the L_1 and L_2 inductor is determined as (18):

$$L_{1,2} = \frac{R_L\left(1-\frac{4\propto}{\pi}-4D_{ST}\right)(D_{ST}+\frac{\propto}{\pi})T}{r_L\%\times f_s} \tag{18}$$

B. Capacitance Selection

From (8), the required capacitances of C_1-C_3 are calculated as (19):

$$\begin{aligned} C_1 &= \frac{\left(1-\frac{\propto}{\pi}-D_{ST}\right)(D_{ST}+\frac{\propto}{\pi})}{\left(1-\frac{4\propto}{\pi}-4D_{ST}\right)R_L\times r_L\%\times f_s} \\ C_2 = C_3 &= \frac{\left(1-\frac{\propto}{\pi}-D_{ST}\right)(D_{ST}+\frac{\propto}{\pi})}{\left(1-\frac{4\propto}{\pi}-4D_{ST}\right)R_L\times r_L\%\times f_s} \end{aligned} \tag{19}$$

$r_{C1}\%$ and $r_{C2,3}\%$ are as (20):

$$\begin{cases} r_{C1}\% = \frac{\Delta V_{C1}}{V_{C1}} \\ r_{C2,3}\% = \frac{\Delta V_{C2}}{V_{C2}} \end{cases} \tag{20}$$

C. COMPARISON

The proposed HG-SCL-ASBI is compared with a similar one and three other inverters such as the EB-ASN-qZSI [29], CSC-EB-ZSI [30], and HG-ZSI [38] in Table I. These comparisons are about the boost factor, the number of components, the capacitors voltages, and the inductors currents. In Table I, the advantages and disadvantages of the HG-SCL-ASBI are shown.

TABLE I
Comparing The Proposed Inverter With Other Inverters

Parameters	Proposed	SCL-ASBI	EB/ASN-qZSI	CSC-EB-ZSI	HG-ZSI
Switch	5	5	5	5	5
Diode	7	7	8	7	8
Inductor	2	2	2	3	2
Capacitor	3	3	2	4	2
Voltage Gain (G)	$\frac{1}{1-\frac{4\propto}{\pi}-4D}$	$\frac{1}{1-4D}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-3D-D^2}$
V_{C1}/V_i V_{C2}/V_i V_{C3}/V_i V_{C4}/V_i	G G/2 G/2 -	G G/2 G/2 -	G (1-2D)G - -	DG (1-2D)G DG DG	G DG - -
I_{L1}/I_{pv} I_{L2}/I_{pv} I_{L3}/I_{pv}	$\frac{(1-\frac{\propto}{\pi}-D)}{(1-4\frac{\propto}{\pi}-4D)}$ - -	(1-D)G (1-D)G -	G (1-D)G -	(1-D) G $(1-D)^2G$ $(1-D)^2G$	(1-D) G $(1-D)^2G$ -

According to Table I, All the structures have the same number of switches. Nonetheless, the EB/ASN-qZSI and HG-ZSI have the lowest number of capacitors and inductors. CSC-EB-ZSI has the greatest number of inductors, and it has the lowest stress of capacitors voltage. HG-SCL-ASBI is the best compared to the other inverters in this table in terms of the voltage gain in the same duty cycle. Unlike the other four inverters, two elements D_{ST} and $\propto$ affect the boosting of the HG-SCL-ASBI. Fig. 6 shows the plots of boost factor of the

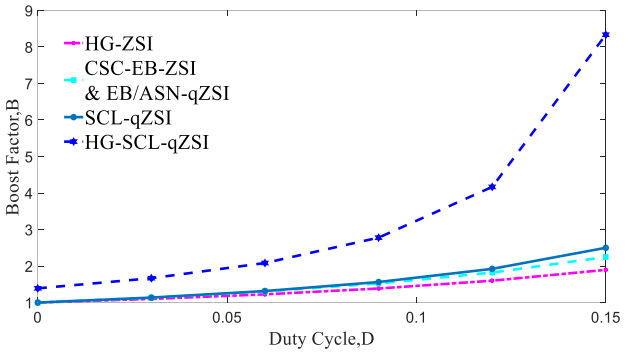

Fig. 6. Boost factors of five topologies.

HG-SCL-ASBI and other topologies in the variation of the duty cycle.

IV. Simulation Results

To confirm the advantages of the introduced structure, we use Matlab/Simulink to simulate it. The simulation parameters are depicted in Table II. Fig. 7 shows the simulation result. The load voltage, V_{load}, and the dc input voltage, V_{pn}, of the H-Bridge are illustrated in Fig.7.a and Fig.7.b, respectively.

According to Fig. 7(d), the voltage of C_1 is 338v and, the voltages of C_2 and C_3 are 149v. In Fig.7(e) and Fig. 7(f), the voltages and currents of diodes are depicted. Fig. 8 illustrates the voltage stresses of S_1-S_4. As it can be seen, the voltage stresses of S_1-S_4 are equal to V_{pn}, Which is shown in Fig. 7(a) In addition, Fig. 8 shows S_1 and S_2 are turned off under ZVS conditions, and S_3 and S_4 are turned on under the ZVS.

TABLE II
Parameters Of HG-SCL-ASBI

Parameters	Values
input voltage (V_i)	40 V
inductors (L_1= L_2)	3 mH
capacitor (C_1)	200 µF
capacitors (C_2 = C_3)	260 µF
Switching frequency (f_{sw})	5 kHz
Modulation index (M)	1
Fundamental frequency (f_o)	5 kHz
∝	10°
D_{ST}	0.15

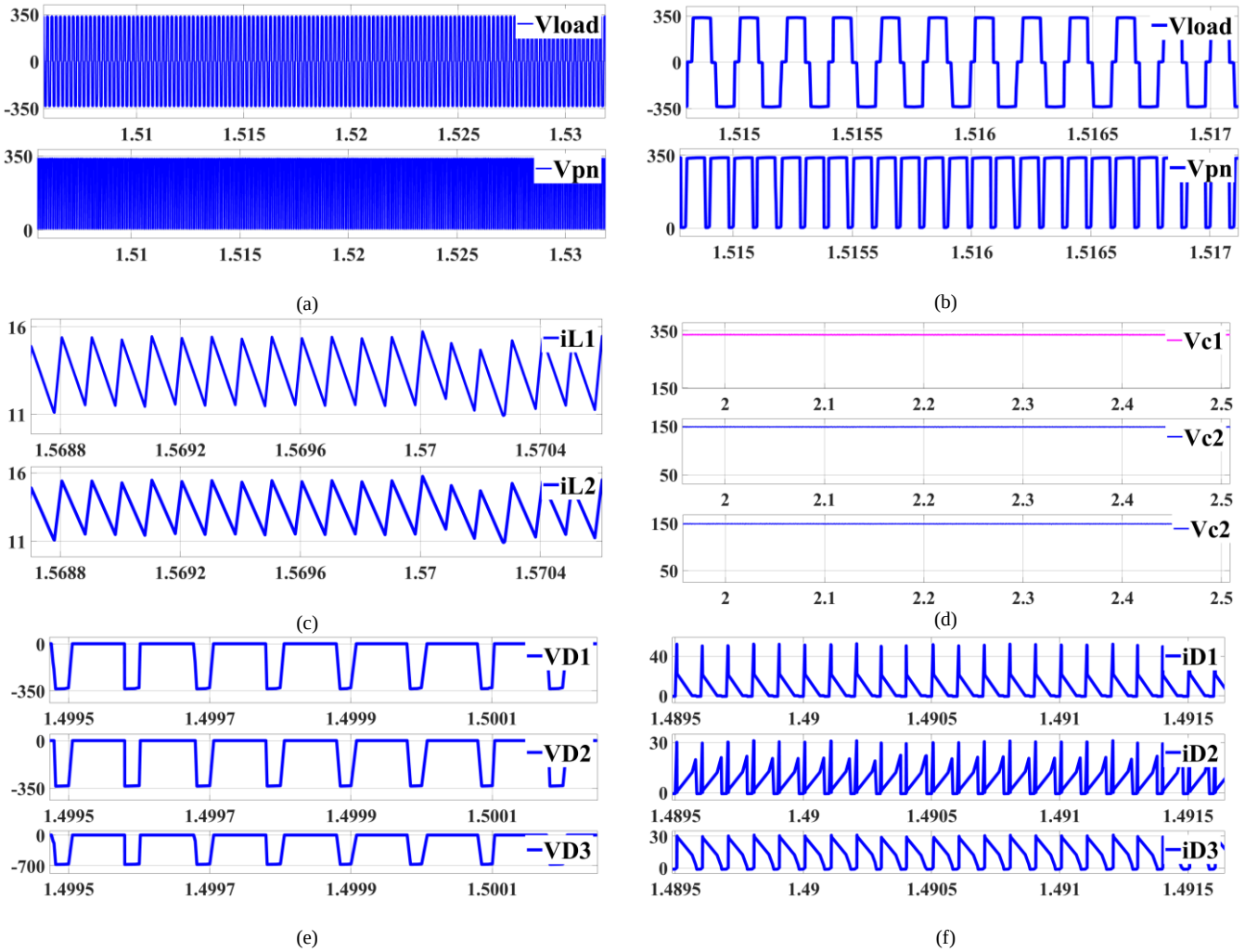

Fig. 7. Simulation results of the proposed inverter, (a) V_{Load}, V_{pn} (b) V_{Load}, V_{pn} (c) i_{L1}, i_{L2} (d) V_{C1}, V_{C2}, V_{C3} (e) V_{D1}, V_{D2}, V_{D3} (f) i_{D1}, i_{D2}, i_{D3}

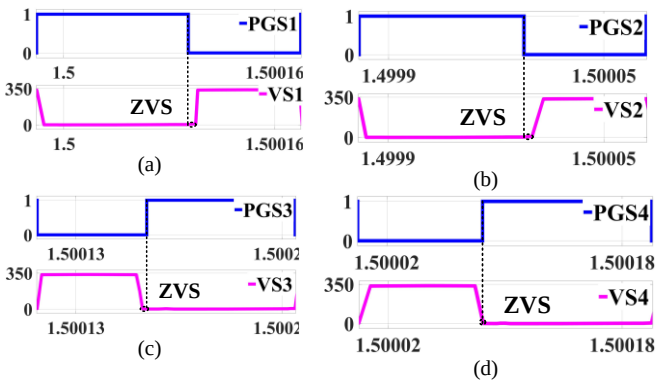

Fig. 8. Switches Pulse and Switches voltage of the, (a) S_1, (b) S_2, (c) S_3, (d) S_4.

V. CONCLUSION

In this article, a new control algorithm is applied to HG-SCL-ASBI. This control method is based on PWM and phase-shift techniques. The SCL- ASBI needs a large duty cycles to provide high boost factor. But, in the proposed HG-SCL-ASBI, the boost factor is improved. This inverter provides high gain with a low duty cycle. The introduced controller improves the boost factor and makes the soft-switching condition for the switches. The HG-SCL-ASBI with introduced controller has the following advantages: high boost factor, soft-switching condition, continuous input current, a small number of elements in the impedance network, high-frequency switching, flexible boost factor, low EMI noises, and shoot through safety. The above features are achieved without adding additional components. In this article, the theoretical analysis and the design guidelines of impedance parameters are discussed. The introduced inverter is compared to the similar SCL-ASBI. Ultimately, the presented steady-state analysis is validated by the simulation result.

VI. REFERENCES

[1] S. Jain and V. Agarwal. (2007, Sep). A Single-Stage Grid Connected Inverter Topology for Solar PV Systems with Maximum Power Point Tracking. *IEEE Trans. Power Electron. 22(5),* pp. 1928–1940.

[2] F.Z. Peng. (2003, Mar-Apr). Z-source inverter. *IEEE Trans. Ind. Appl. 39(2),* pp.504–510.

[3] J. Anderson and F.Z. Peng, "Four quasi-Z source inverters," in *PESC Record—IEEE ann. power electron. spec. conf.*, 2008, pp. 2743–2749.

[4] P.C. Loh, F. Gao, and F. Blaabjerg. (2010, Jan-Feb). Embedded EZ-source inverters. *IEEE Trans. Power Electron. 46(1),* pp. 256–267.

[5] M. Abbasi and E. Babaei, "A new topology of embedded Z-source inverter with low voltage stress on capacitors," in *2016 13th Int. Conf. Electr. Eng./Electron. Comput. Telecommun. Inf. Technol. (ECTI-CON),* 2016.

[6] J. Anderson and F. Z. peng, "A class of quasi-Z-source inverters," in *Proc.Conf. Rec. IEEE-IAS Annu. Meeting,* 2008, pp. 1–7.

[7] M. K. Nguyen, Y. C. Lim, and S. J. Park. (2015, Oct). A comparison between single-phase quasi-Z-source, and quasi-switched boost inverters. *IEEE Trans. Ind. Electron. 62(10),* pp. 6336–6344.

[8] H. Abu-Rub, A. Iqbal, S. M. Ahmed, F. Z. Peng, Y. Li, and G. Baoming. (2013, Jan). Quasi-Z-source inverter-based photovoltaic generation system with maximum power tracking control using ANFIS. *IEEE Trans. Power Electron. 4(1),* pp. 11–20.

[9] Y. Li, B. Ge, H. Abu-Rub, and F. Z. Peng. (2014, Feb). An effective control method for quasi-Z-source cascade multilevel inverter-based grid-tie single-phase photovoltaic power system. *IEEE Trans. Ind. Informat. 10(1),* pp. 399–407.

[10] Y. Zhou, L. Liu, and H. Li. (2013, Jun). A high-performance photovoltaic module integrated converter (MIC) based on cascaded quasi-Z-source inverters(qZSI) using eGaN FETs. *IEEE Trans. Power Electron. 28(6),* pp. 2727–2738.

[11] F. Guo, L. Fu, C. H. Lin, C. Li, W. Choi, and J. Wang. (2013, Dec). Development of an 85-kW bidirectional quasi-Z-source inverter with DC-link feed-forward compensation for electric vehicle applications. *IEEE Trans. Power Electron. 28(12),* pp. 5477–5488.

[12] Q. Lei, D. Cao, and F. Z. Peng. (2014, Mar). Novel loss and harmonic minimized vector modulation for a current-fed quasi-Z-source inverter in HEV motor drive application. *IEEE Trans. Power Electron. 29(3),* pp. 1344–1357.

[13] M. K. Nguyen, Y. C. Lim, and G. B. Cho. (2011, Nov). Switched-inductor quasi- Z-source inverter. *IEEE Trans. Power Electron. 26(11),* pp. 3183–3191.

[14] M. Zhu, K. Yu, and F. L. Luo. (2010, Aug). Switched-inductor Z-source inverter. *IEEE Trans. Power Electron. 25(8),* pp. 2150–2158.

[15] C. J. Gajanayake, L. F. Lin, G. H. Beng, S. P. Lam, and S. L. Kian, "Extended boost Z-source inverters," in *2009 IEEE Energy Convers. Congr. Expo. ECCE,* 2009, pp 3845–3852.

[16] M. K. Nguyen, Y. C. Lim, and G. B. Cho. (2011, Nov). Switched-inductor quasi-Z-source inverter. *IEEE Trans. Power Electron. 26(11),* pp. 3183–3191.

[17] M. Zhu, K. Yu and F. L. Luo. (2010, Aug). Switched-inductor Z-source inverter. *IEEE Trans. Power Electron. 25(8),* pp. 2150–2158.

[18] M. K. Nguyen, Y. C. Lim and J. H. Choi. (2012, Aug). Two switched-inductor quasi- Z-source inverters. *IET Power Electron. 5(7),* pp. 1017–1025.

[19] H. Fathi and H. Madadi. (2016, Feb). Enhanced-boost Z-source inverters with switched Z-impedance. *IEEE Trans. Ind. Electron. 63(2),* pp. 691–703.

[20] V. Jagan, J. Kotturu and S. Das. (2017, Sep). Enhanced-boost quasi-Z-source inverters with two-switched impedance networks. *IEEE Trans. Ind. Electron. 64(9),* pp. 6885–6897.

[21] J. Abbasi Bolaghi, A. Taheri, M. H. Babaei, and M. Gholami. (2021, Dec). Quasi Z-source inverter with switched-capacitor-inductor for enhancing boost factor. *IET Power Electron. 14(16),* pp. 2545–2562.

[22] J. Abbasi Bolaghi, A. Taheri, and M. H. Babaei. (2021, May). Switched-capacitor inductor Z-source inverter with an impedance network. *Int. Trans. Electr. Energ. Syst. 31(5),* pp. e12529.

[23] X. Zhu, B. Zhang and D. Qiu. (2019, Sep). A new nonisolated quasi-Z-source inverter with high voltage gain. *IEEE J. Emerg. Sel. Topics Power Electron. 7(3),* pp. 2012–2028.

[24] A. Karbalaei and m. mardaneh. (2021, Jan). Uplifted-Boost switched-Inductor/Capacitor Quasi Z-Source Inverter. *IEEE Ind. Electron. Mag.*

[25] A. Ho, T. Chun, and H. Kim. (2015, Oct). Extended Boost Active-Switched-Capacitor/Switched-Inductor Quasi-Z-Source Inverters. *IEEE Trans. Power Electron. 30(10),* pp. 5681–5690.

[26] A. Ahmad, R. K. Singh and A. R. Beig. (2019, Dec). Switched-capacitor based modified extended high gain switched boost Z-source inverters. *IEEE Access. 7,* pp. 179918–179928.

[27] Y. Gu, Y. Chen, and B. Zhang. (2018, Oct). Enhanced-boost quasi-Z-source inverter with an active switched Z-network. *IEEE Trans. Ind. Electron. 65(10),* pp. 8372–8381.

[28] X. Zhu, B. Zhang, and D. Qiu. (2018, Sep). Enhanced boost quasi-Z-source inverters with active switched-inductor boost network. *IET Power Electron. 11(11),* pp. 1774–1787.

[29] X. Zhu, B. Zhang, and D. Qiu. (2019, Sep). A High Boost Active Switched Quasi-Z-Source Inverter With Low Input Current Ripple. *IEEE Trans. Industr. Inform. 15(9),* pp. 5341–5354.

[30] M. Abbasi, M. Mardaneh, and E. Jamshidpour. (2022, Feb). High Gain PWM Method and Active Switched Boost Z-Source Inverter With Less Voltage Stress on the Devices. *IEEE Trans. Power Electron. 37(2),* pp. 1841–1851.

[31] A. Ravindranath, S. K. Mishra and A. Joshi. (2013, Dec). Analysis and PWM control of switched boost inverter. *IEEE Trans. Ind. Electron. 60(12),* pp. 5593–5602.

[32] S. S. Nag and S. Mishra. (2014, Sep). Current-fed switched inverter. *IEEE Trans. Ind. Electron. 61(9),* pp. 4680–4690.

[33] M. Nguyen, T. Duong, Y. Lim, and J. Choi. (2019, Sep). High Voltage Gain Quasi-Switched Boost Inverters With Low Input Current Ripple. *IEEE Trans. Industr. Inform. 15(9),* pp. 4857–4866.

[34] A. Kumar, D. Bao, and A. R. Beig. (2021, Apr). Comparative Analysis of Extended SC-qSBI With EB-QZSI and EB/ASN-QZSI. *IEEE Access. 9*, pp. 61539-61547.

[35] Z. Mokhtari and A. Asghari, "High Step up Switched-Capacitor Quasi-Switched Boost Inverters," in *2021 12th Power Electron. Drive Syst. Technol. Conf. (PEDSTC)*, 2021.

[36] A. T. Huynh, A. V. Ho, and T. W. Chun. (2021, Jul). Switched-Capacitor-Inductor Active-Switched Boost Inverters With High Boost Ability. *IEEE Access. 9*, pp. 101543–101554.

[37] M. Nguyen, T. Tran, and Y. Lim. (2019, Feb). A Family of PWM Control Strategies for Single-Phase Quasi-Switched-Boost Inverter. *IEEE Trans. Power Electron. 34(2)*, pp. 1458–1469.

[38] M. H. Babayi Nozadian, E. Babaei, S. H. Hosseini, and E. Shokati Asl. (2017, Jul). Steady-State Analysis and Design Considerations of High Voltage Gain Switched Z-Source Inverter with Continuous Input Current. *IEEE Trans. Ind. Electron. 64(7)*, pp. 5342–5350.